800G OSFP DR8/DR8+ Optical Transceiver

Jabil 800Gb/s OSFP DR8/DR8+ (Data Center Reach 8-lane) Optical Transceiver is a small form-factor, high speed, and low power consumption product targeted for use in optical interconnects for data communications applications. The high bandwidth module supports dual 400G Ethernet connections, octal 100G Ethernet connections, or a single 800G Ethernet connection over parallel single-mode fiber links up to 2 km. The module also can be configured via software control for half-rate operation as a 400G (400GbE, 2x200GbE breakout, or 8x50GbE breakout) optical transceiver for applications that require backwards compatibility.

FEATURES

- Compliant with 2x IEEE 400GBASE-DR4 optical interface standard and 8x IEEE 802.3cu 100G-FR1 optical interface specification for use in 800G, 2x400G breakout, or 8x100G breakout applications up to 2 km, plus selectable half-rate mode to support operation as a 400G/2x200G/8x50G optical transceiver.
- Compliant to IEEE 802.3df
- Electrical interface compliant with 2x IEEE 802.3ck 400GAUI-4 standard
- OSFP form-factor for high faceplate density in networking equipment Dual MPO-12 connector for single-mode parallel cable infrastructures
- Typical power dissipation of 15W, compliant with OSFP power envelope
- Operating temperature range: 0° to 70°C
- CMIS-compliant management interface with full module diagnostics and control through I2C

APPLICATIONS

- 800GbE connectivity, 2x400GbE breakout connectivity, or 8x100GbE breakout connectivity for large-scale cloud and enterprise data centers
- Ethernet switch, router, and client-side telecom interfaces

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Storage Temperature	Ts	-40	+85	ºC
Case Temperature (Powered)	Tc	-5	75	ºC
Relative Humidity (*)	RH	5	85	%
Power Supplies	V_{CC}	-	3.6	V
ESD (HBM)	V_{ESD}	-1k	1k	V
Differential Input Voltage	$V_{in\text{-}pp}$	-	1600	mVpp
Receiver Input Optical Power	P_{in} (max)	-	+3.5	dBm

(*) not condensing

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Operating Case Temperature	Tc	0	30	70	°C
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V
Power Supply Noise Tolerance (*)		-	-	50	mVpp
Bit Rate	BR	106.24	106.25	106.26	Gbps

(*) At input to recommended power supply filter

Optical Transmitter

The 800G DR8/DR8+ optical transceiver electrical interface is based on (2x of) the IEEE 802.3ck 400GAUI-4 host to module retimed interface (per IEEE 802.3ck Annex 120G). The 800G DR8/DR8+ optical transmitter is compliant with (2x of) the IEEE 802.3bs 400GBASE-DR4 specification on eight channels of 100G PAM4 data on parallel single-mode fiber (100G per fiber), with additional optical reach of up to 2 km. Each optical lane is compliant with the 100G Lambda MSA 100G FR optical interface specification. The DR4 and FR1 optical interface standards are defined assuming IEEE standard 400G KP4 RS(544,514) forward error correction (FEC) implemented in the host or switch equipment in order to enable error-free link operation.

100G/lane specifications are shown below; the 800G DR8/DR8+ optical transceiver also supports a software-configurable 50G/lane mode (8x50G PAM4) for backwards compatibility.

TRANSMITTER ELECTRICAL INPUT CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Data modulation type			PAM4		
Data rate, each lane	BR	106.24	106.25	106.26	Gbps
Baud/symbol rate, each lane	BR		53.125 ± 100ppm		Gbd
Differential pk-pk voltage tolerance		750	-	-	mV
AC common-mode RMS voltage tolerance		25	-	-	mV
Differential-mode to common-mode return loss			as per 802.3ck 120G-2		
Effective return loss, ERL		8.5	-	-	dB
Differential termination mismatch		-	-	10	%
Module stressed input tolerance			as per 802.3ck 120G.3.4.3		
Single-ended voltage tolerance	V_{in_SE}	-0.4	-	3.3	V
DC common-mode voltage tolerance		-0.35	-	2.85	V

TRANSMITTER OPTICAL OUTPUT CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data modulation type			PAM4			
Data rate, each lane	BR	106.24	106.25	106.26	Gbps	
Baud/symbol rate, each lane	BR	53.12	53.125	53.13	Gbd	
Lane wavelength range	WL	1304.5	1311	1317.5	nm	
Side mode suppression ratio	SMSR	30	-	-	dB	
800G DR8+ (2KM PRODUCT VARIANT) – EACH LANE						
Average optical output power	P_{ave}	-3.1	-	4	dBm	
Optical modulation amplitude	OMA_{outer}	-	-	4.2	dBm	
OMA for TDECQ ≤ 1.4dB		-0.1	-	-	dBm	
OMA for 1.4dB ≤ TDECQ ≤ 3.4dB		-1.5+TDECQ	-	-	dBm	
Transmitter dispersion and eye closure penalty	TDECQ	-	-	3.4	dB	
|TDECQ-TECQ|		-	-	2.5	dBm	
Over/under-shoot		-	-	22	%	
Transmitter power excursion		-	-	2	dBm	
Extinction ratio	ER	3.5	-	-	dB	
Transmitter transition time		-	-	17	ps	
Average optical output power of OFF transmitter		-	-	-15	dBm	
$RIN_{17.1}$ OMA	RIN	-	-	-136	dB/Hz	
Optical return loss tolerance	ORLT	-	-	17.1	dB	
Transmitter reflectance		-	-	-26	dB	1
Operating link reach		2	-	2000	m	

TRANSMITTER OPTICAL OUTPUT CHARACTERISTICS CONT.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
800G DR8 (500M PRODUCT VARIANT) – EACH LANE						
Average optical output power	P_{ave}	-2.9	-	4	dBm	
Optical modulation amplitude	OMA_{outer}	-	-	4.2	dBm	
OMA for TDECQ < 1.4dB		-0.8	-	-	dBm	
OMA for 1.4dB < TDECQ < 3.4dB		-2.2 + TDECQ	-	-	dBm	
Launch power in OMA minus TDECQ		-1.9	-	-	dBm	
Transmitter dispersion and eye closure penalty	TDECQ	-	-	3.4	dB	
TDECQ-$10\log_{10}(C_{eq})$		-	-	3.4	dBm	
Extinction ratio	ER	3.5	-	-	dB	
Transmitter transition time		-	-	17	ps	
Average optical output power of OFF transmitter		-	-	-15	dBm	
$RIN_{15.5}OMA$	RIN	-	-	-136	dB/Hz	
Optical return loss tolerance	ORLT	-	-	15.5	dB	
Transmitter reflectance		-	-	-26	dB	1
Operating link reach		2	-	500	m	

(1) Transmitter reflectance is defined looking into the transmitter

Optical Receiver

The 800G DR8/DR8+ optical transceiver electrical interface is based on (2x of) the IEEE 802.3ck 400GAUI-4 host to module retimed interface (per IEEE 802.3ck Annex 120G). The 800G DR8/DR8+ optical receiver is compliant with (2x of) the IEEE 802.3bs 400GBASE-DR4 standard on 8 channels of 100G PAM4 data on parallel single-mode fiber (100G per fiber), with additional optical reach of up to 2 km. Each optical lane is compliant with the IEEE 802.3cu 100G-FR1 optical interface specification. The DR4 and FR1 optical interface standards are defined assuming IEEE standard 400G KP4 RS(544,514) forward error correction (FEC) implemented in the host or switch equipment in order to enable error-free link operation.

100G/lane specifications are shown below; the 800G DR8/DR8+ optical transceiver also supports a software-configurable 50G/lane mode (8x50G PAM4) for backwards compatibility.

RECEIVER ELECTRICAL OUTPUT CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Data modulation type			PAM4		
Data rate, each lane	BR	106.24	106.25	106.26	Gbps
Baud/symbol rate, each lane	BR	53.12	53.125	53.13	Gbd
Peak-to-peak AC common-mode voltage, short mode		-	-	60	mV
Peak-to-peak AC common-mode voltage, long mode		-	-	80	mV
Differential peak-to-peak output voltage, short mode		-	-	600	mV
Differential peak-to-peak output voltage, long mode		-	-	845	mV
Eye height		15	-	-	mV
Vertical eye closure	VEC	-	-	12	dB
Common-mode to differential-mode return loss			as per 802.3ck 120G-1		
Effective return loss	ERL		8.5		dB
Differential termination mismatch		-	-	10	%
Transition time (20-80%)	T_{rf}	TBD	-	8.5	ps

RECEIVER OPTICAL INPUT CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data modulation type			PAM4			
Data rate, each lane	BR	106.24	106.25	106.26	Gbps	
Baud/symbol rate, each lane	BR	53.12	53.125	53.13	Gbd	
Lane wavelengths	WL	1304.5	1311	1317.5	nm	
Bit Error Rate, uncorrected/pre-FEC	BER_{pre}	-	-	2×10^{-4}		
Bit Error Rate, corrected/post-FEC	BER_{post}	-	-	1×10^{-15}		
800G DR8+ (2 KM PRODUCT VARIANT) – EACH LANE						
Damage threshold		-	-	5	dBm	1
Average receive power		-7.1	-	4	dBm	
Receive power in OMA_{outer}		-	-	4.2	dBm	
Receiver reflectance		-	-	-26	dB	
Unstressed receiver sensitivity (OMA_{outer}), for TECQ < 1.4dB, at pre-FEC BER of 2×10^{-4}	URS	-	-	-4.5	dBm	2
Unstressed receiver sensitivity (OMA_{outer}), for 1.4dB ≤TECQ ≤ 3.4dB, at pre-FEC BER of 2×10^{-4}	URS	-	-	-5.9+TECQ	dBm	2
Stressed receiver sensitivity (OMA_{outer}), at pre-FEC BER of 2×10^{-4}	SRS	-	-	-2.5	dBm	

RECEIVER OPTICAL INPUT CHARACTERISTICS CONT.

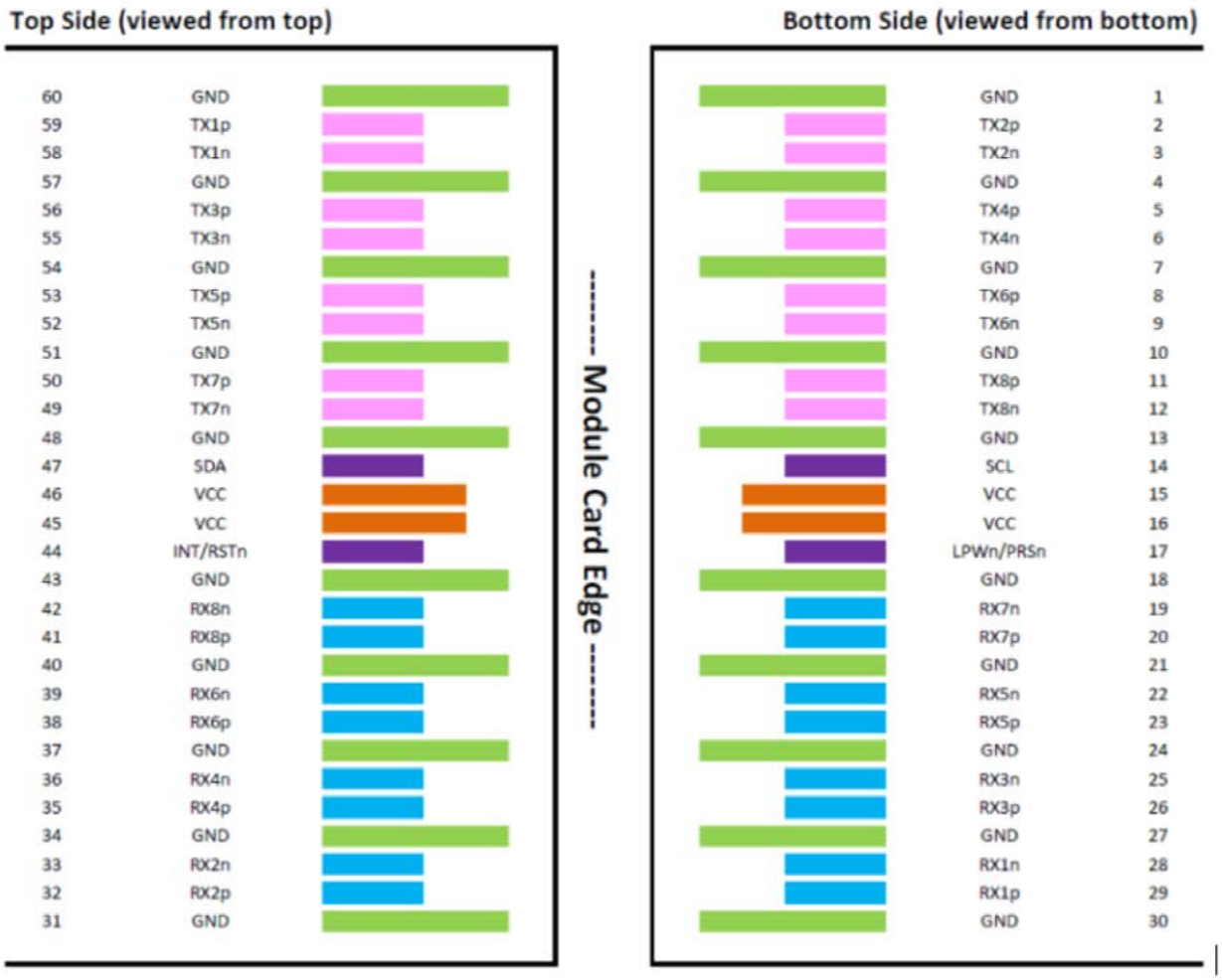
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
800G DR8 (500 M PRODUCT VARIANT) – EACH LANE						
Damage threshold		-	-	5	dBm	1
Average receive power		-5.9	-	4	dBm	
Receive power in OMA_{outer}		-	-	4.2	dBm	
Receiver reflectance		-	-	-26	dB	
Unstressed receiver sensitivity (OMA_{outer}), at pre-FEC BER of 2×10^{-4}	URS	max(-3.9, SECQ-5.3)			dBm	2
Stressed receiver sensitivity (OMA_{outer}), at pre-FEC BER of 2×10^{-4}	SRS	-	-	-1.9	dBm	
CONDITIONS OF STRESSED RECEIVER SENSITIVITY TEST						
Stressed eye closure for PAM4 (SECQ)	SECQ	3.4			dB	3

(1) The receiver is able to tolerate, without damage, continuous exposure to a signal having this average optical power level.
(2) Unstressed receiver sensitivity is informative and is defined via the equation given for a test transmitter SECQ up to 3.4 dB.
(3) These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Electrical PIN Assignment

The 800G optical transceiver pinout is compliant with the OSFP MSA specifications. The figure below shows the module connector pad layout, and the table below lists and describes all the electrical pins of the module.

ELECTRICAL CONNECTOR PAD LAYOUT



OSFP MODULE ELECTRICAL CONNECTOR PIN DEFINITIONS

PAD	SYMBOL	DESCRIPTION	LOGIC	DIRECTION	PLUG SEQUENCE	NOTES
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial Iinterface Cclock	LVCMOS-I/O	Bi-directional	3	Open drain with pullup resistor on host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	

OSFP MODULE ELECTRICAL CONNECTOR PIN DEFINITIONS CONT.

PAD	SYMBOL	DESCRIPTION	LOGIC	DIRECTION	PLUG SEQUENCE	NOTES
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC	+3.3V Power		Power from Host	2	

OSFP MODULE ELECTRICAL CONNECTOR PIN DEFINITIONS CONT.

PAD	SYMBOL	DESCRIPTION	LOGIC	DIRECTION	PLUG SEQUENCE	NOTES
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial Iinterface Ddata	LVCMOS-I/O	Bi-directional	3	Open drain with pullup resistor on host
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

Power Supply

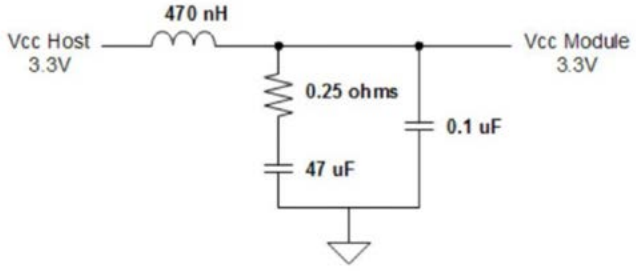
Here we describe the power supply filtering requirements and the power supply sequencing requirements.

POWER SUPPLY FILTERING

The power supply filtering requirements for the 800G DR8/DR8+ OSFP Optical Transceiver have been designed to be consistent with those required for OSFP modules. A representative power supply filtering circuit for use on the host board is shown in the figure below.

One filtering circuit is recommended for each power supply rail.

RECOMMENDED POWER SUPPLY FILTERING CIRCUIT



POWER SUPPLY SPECIFICATIONS

Power supply specifications for the module are defined below. The module is compliant with OSFP Power Class 8.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power supply voltages VccTx, VccTx1, VccRx, VccRx1, Vcc1, and Vcc2 (*)	VCC	3.135	3.3	3.465	V
Host RMS noise output 10 Hz – 10 MHz		-	-	25	mV
Module RMS noise output 10 Hz – 10 MHz		-	-	15	mV
Module power supply noise tolerance 10 Hz – 10 MHz (peak-to-peak)	$PSNR_{mod}$	-	-	66	mV
Module inrush – instantaneous peak duration	T_ip	-	-	50	µs
Module inrush – initialization time	T_init	-	-	500	ms
Inrush and discharge current	I_didt	-	-	100	mA/µs
High power to low power mode transition time (**)	T_hplp	-	-	200	µs

(*) Measured including ripple, droop, and noise below 100 kHz.

(**) From assertion of M_LPWn or M_RSTn or ForceLowPwr. I_didt will not be exceeded for any power transient events, including hot plug/unplug, power up/down, initialization, low-power to high-power and high-power to low-power transitions.

LOW POWER MODE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power consumption	P_1	-	-	1.5	W
Instantaneous peak current at hot plug	Icc_ip_1	-	-	600	mA
Sustained peak current at hot plug	Icc_sp_1	-	-	495	mA
Steady state current	Icc_lp	-	-	478	mA

HIGH POWER MODE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power consumption	P_8	-	15	16	W
Instantaneous peak current at hot plug	Icc_ip_8	-	-	6400	mA
Sustained peak current at hot plug	Icc_sp_8	-	-	5328	mA
Steady state current	Icc_8	-	-	5104	mA

POWER SUPPLY SEQUENCING

No host power supply sequencing is required.

Control and Monitoring Interface

The optical transceiver supports a full CMIS-compliant set of control, alarm, and monitoring features through a standard I²C management interface, as well as low speed control pins, which support additional module control and interrupt features.

LOW SPEED ELECTRICAL HARDWARE INTERFACE

In addition to the I²C interface, the optical transceiver also supports low speed control pins, which provide immediate easy access to key module functions and provide additional user interface signals to support the management interface.

INT/RSTn

INT/RSTn is a dual-function signal that allows the module to raise an interrupt to the host and allows the host to reset the module. The host circuit enables multi-level signaling to provide direct signal control in both directions. Reset is an active low signal on the host, which is translated to an active-low signal on the module. Interrupt is an active high signal on the module, which gets translated to an active low signal on the host.

The INT/RSTn signal operates in three voltage zones to indicate the state of reset for the module and interrupt for the host:

- **Zone 1 (reset operation):** Module in reset, interrupt deasserted (M_RSTn=Low, H_INTn=High). See table below for min/max voltages for Zone 1.
- **Zone 2 (normal operation):** Reset deasserted (M_RSTn=High) and interrupt deasserted (H_INTn=High). See table below for min/max voltages for Zone 2.
- **Zone 3 (interrupt operation):** Module out of reset and interrupt asserted (M_RSTn=High, H_INTn=Low). See table below for min/max voltages for Zone 3.

The table below shows voltage ranges for these three zones. The host uses a voltage reference at 2.5 volts to determine the state of the H_INTn signal, and the module uses a voltage reference at 1.25V to determine the state of the M_RSTn signal.

PARAMETER	MIN	NOMINAL	MAX	UNITS	NOTE
Host VCC	3.135	3.300	3.465	Volts	VCC voltage on the host
H_Vref_INTn	2.475	2.500	2.525	Volts	Precision voltage reference for H_INTn
M_Vref_RSTn	1.238	1.250	1.263	Volts	Precision voltage reference for M_RSTn
R1	66k	68k	70k	Ohms	Recommend 68.1k Ω 1% resistor
R2	4.9k	5k	5.1k	Ohms	Recommend 4.99k Ω 1% resistor
R3	7.8k	8k	8.2k	Ohms	Recommend 8.06k Ω 1% resistor
V_INT/RSTn_1	0.000	0.000	1.000	Volts	Zone 1: INT/RSTn voltage for no module
V_INT/RSTn_2	0.000	0.000	1.000	Volts	Zone 1: INT/RSTn voltage for module installed, H_RSTn=Low
V_INT/RSTn_3	1.500	1.900	2.250	Volts	Zone 2: INT/RSTn voltage for module installed, H_RSTn=High, M_INT=Low
V_INT/RSTn_4	2.750	3.000	3.465	Volts	Zone 3: INT/RSTn voltage for module installed, H_RSTn=High, M_INT=High

LPWn/PRSn

LPWn/PRSn is a dual-function signal that allows the host to signal Low Power mode and the module to indicate Module Present. The host circuit enables multilevel signaling to provide direct signal control in both directions. Low Power mode is an active low signal on the host, which gets converted to an active low signal on the module. Module Present is controlled by a pull-down resistor on the module which gets converted to an active low logic signal on the host.

The LPWn/PRSn signal operates in three voltage zones to indicate the state of Low Power mode for the module and Module Present for the host:

- **Zone 1 (low power mode):** Module present and in low power mode (M_LPWn=Low, H_PRSn=Low). See table below for min/max voltages for Zone 1.
- **Zone 2 (high power mode):** Module present and in high power mode (M_LPWn=High, H_PRSn=Low). See table below for min/max voltages for Zone 2.
- **Zone 3 (module not present):** Module not present (H_PRSn=High). See table below for min/max voltages for Zone 3.

The table below shows voltage ranges for these three zones. The host uses a voltage reference at 2.5 volts to determine the state of the H_PRSn signal and the module uses a voltage reference at 1.25V to determine the state of the M_LPWn signal.

If the module is being unplugged and LPWn/PRSn loses contact, the pull-down resistor on the host will assert Low Power mode on the module (M_LPWn=Low), at which point the module will transition to low power (Power Class 1) and disable transmitters within the time specified by T_hplp.

The LPWn/PRSn signal is driven high or open by the host for Low Power mode control. If logic is used to generate the high level, then 3.3V LVCMOS is preferred.

The module transmitters are disabled when in low power mode. In addition, a software-controlled transmitter disable is provided by the TX Disable register via the I2C interface.

PARAMETER	MIN	NOMINAL	MAX	UNITS	NOTE
Host VCC	3.135	3.300	3.465	Volts	VCC voltage on the Host
H_Vref_PRSn	2.475	2.500	2.525	Volts	Precision voltage reference for H_PRSn
M_Vref_LPWn	1.238	1.250	1.263	Volts	Precision voltage reference for M_LPWn
R11	24.5k	25k	25.5k	Ohms	Recommend 24.9k ohms 1% resistor
R12	14.7k	15k	15.3k	Ohms	Recommend 15k ohms 1% resistor
R13	9.8k	10k	10.2k	Ohms	Recommend 10k ohms 1% resistor
V_LPWn/PRSn _1	0.000	0.950	1.100	Volts	Zone 1: LPWn/PRSn voltage for module installed, H_LPWn=Low
V_LPWn/PRSn _2	1.400	1.700	2.250	Volts	Zone 2: LPWn/PRSn voltage for module installed, H_LPWn=High
V_LPWn/PRSn_3	2.750	3.300	3.465	Volts	Zone 3: LPWn/PRSn voltage for no module
V_INT/RSTn_4	2.750	3.000	3.465	Volts	Zone 3: INT/RSTn voltage for module installed, H_RSTn=High, M_INT=High

SCL

The SCL pin (LVCMOS-I/O open-drain signal) is the 2-wire serial interface clock for the module. The SCL signal requires a pull-up resistor on the host board, between 1 kΩ and 4.7 kΩ depending on capacitive load. Note that SCL and SDA timing specifications are defined in section “Management Interface Timing.”

SDA

The SDA pin (LVCMOS-I/O open-drain signal) is the 2-wire serial interface data for the module. The SDA signal requires a pull-up resistor on the host board, between 1 kΩ and 4.7 kΩ depending on capacitive load. Note that SCL and SDA timing specifications are defined in section “Management Interface Timing.”

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
SCL and SDA	VOL	0	0.4	V	IOL_{max} = 3 mA
	VOH	Vcc-0.5	Vcc+0.3		
	VIL	-0.3	Vcc*0.3		
	VIH	Vcc*0.7	Vcc+0.5		
Capacitance for SCL and SDA I/O signal	Ci	-	14	pF	
Total bus capacitive load for SCL and SDA	Cb	-	100	pF	For 400 kHz clock frequency, max 3 kΩ pull up resistor
		-	200		For 400 kHz clock frequency, max 1.6 kΩ pull up resistor

Management Interface

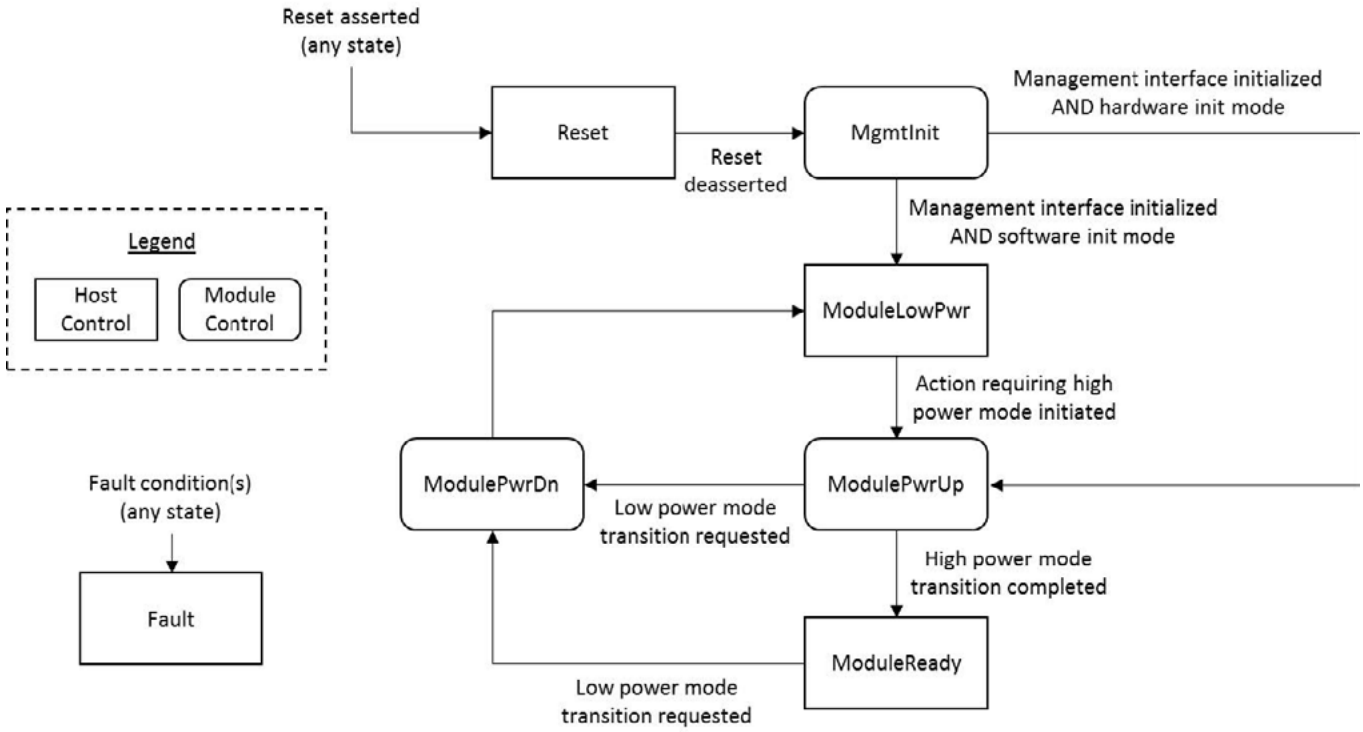
GENERAL FUNCTIONALITY

An I2C interface shall be used for management interface between the optical transceiver and the host system. The communication protocol shall follow the industry standard Common Management Interface Specification (CMIS). Additional detail and clarified functionality are described in this sub-section.

MODULE STATE MACHINES

The module behavior during power-up, mode changes, and fault conditions complies with the Common Management Interface Specification (CMIS), as outlined in the state machine diagrams and descriptions below.

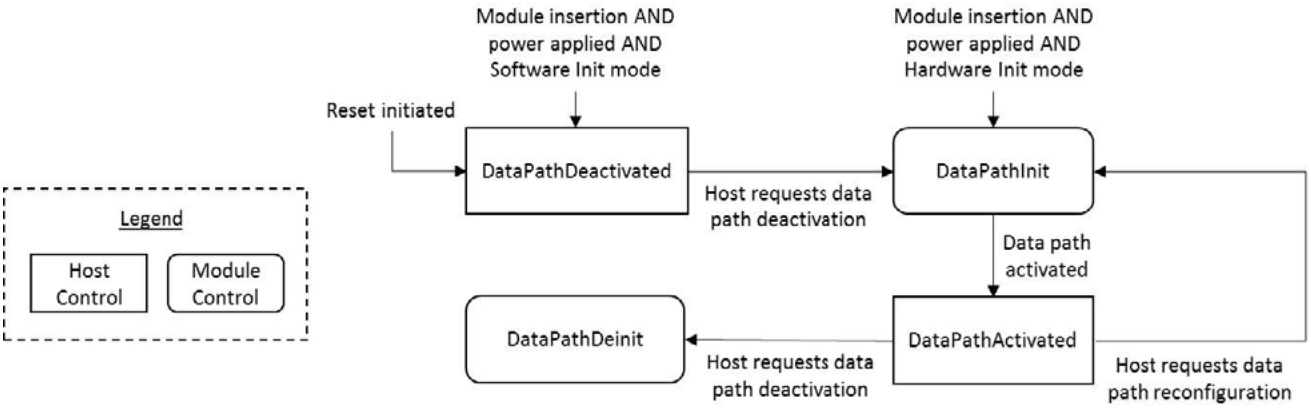
MODULE STATE MACHINE:



MODULE STATES BEHAVIORS

STATE	POWER MODE	EXIT CONDITION	INTERRUPT CLASS	DATA PATH STATE
Reset	Low power	Reset signal deasserted	Suppress all	DataPathDeactivated
MgmtInit	Low power	Module management interface ready AND interrupt signal asserted OR 2s timeout	Suppress all	DataPathDeactivated
ModuleLowPwr	Low power	Host requests an action that requires high power mode	All module flags permitted	DataPathDeactivated
ModulePwrUp	High power	Power up activities are complete	Suppress all	DataPathInit
ModuleReady	High power	Host requests module return to low power mode	All module flags permitted	Varies
ModulePwrDn	High power	Module has returned to low power mode	Suppress all	DataPathDeinit
Fault	Low power	Module reset or power down		DataPathDeactivated

MODULE DATA PATH STATE MACHINE



DATA PATH STATE BEHAVIORS

STATE	TX OUTPUT STATE	RX OUTPUT STATE	INTERRUPT CLASS	EXIT CONDITION
DataPathDeactivated	Quiescent	Quiescent	Suppress all data path flags	Host sets DataPathPwrUp bit(s)
DataPathInit	Quiescent	Quiescent	Suppress all	Module completes data path power up and initialization
DataPathActivated	See Byte 54h	Active	All data path flags permitted	1) Host clears DataPathPwrUp bit(s) AND module is active 2) Host requests data path reconfiguration
DataPathDeinit	Quiescent	Quiescent	Suppress all	Data path decommissioning complete

MANAGEMENT INTERFACE (I²C) TIMING

Timing and other specs for the I2C communication/management interface are given in the table below.

		FAST MODE		FAST MODE +			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNIT	CONDITIONS
Clock Frequency	fSCL	0	400	0	1000	kHz	
Clock Pulse Width Low	tLOW	1.3		0.50		µs	
Clock Pulse Width High	tHIGH	0.6		0.26		µs	
Time bus free before new transmission can start	tBUF	20		1		µs	Between STOP and START and between ACK and Restart
START Hold Time	tHD.STA	0.6		0.26		µs	Delay required between SCL becoming low and SDA starting to go low in a START
START Setup Time	tSU.STA	0.6		0.26		µs	Delay required between SCL becoming high and SDA starting to go low in a START
Data In Hold Time	tHD.DAT	0		0		µs	
Data In Setup Time	tSU.DAT	0.1		0.1		µs	
Input Rise Time	tR		300		120	ns	From VIL to VIH
Input Fall Time	tF		300		120	ns	From VIH to VIL
STOP Setup Time	tSU.STO	0.6		0.26		µs	
STOP Hold Time	tHD.STO	0.6		0.26		µs	
Aborted sequence – bus release	Deselect_ Abort	2		2		ms	Delay from a host deasserting ModSelL (at any point in a bus sequence) to the module releasing SCL and SDA
ModSelL Setup Time	tSU.ModSelL	2		2		ms	Setup time on the select lines before the start of a host initiated serial bus sequence
ModSelL Hold Time	tHD.ModSelL	2		2		ms	Delay from completion of a serial bus sequence to changes of module select status
Serial Interface Clock Holdoff “Clock Stretching”	T_clock_hold		500		500	µs	Maximum time the module may hold the SCL line low before continuing with a read or write operation
Complete Single or Sequential Write	tWR		40		40	ms	Complete (up to) 4 byte write
Endurance (Write Cycles)		50k		50k		cycles	Module case temperature = 70 C

SOFT CONTROL, ALARM, AND STATUS TIMING

Timing specifications for control inputs and alarm/warning and status indicators are described below. Note that alarm and warning flag thresholds are defined in the respective memory map registers, and the Tx Fault and Rx LOS behavior is outlined in the Fault Behavior section.

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITIONS
MgmtInitDuration			2000	ms	Time from power on (*), hot plug, or rising edge of reset until completion of MgmtInit state
ResetL Assert Time	t_reset_init	10		µs	Minimum pulse time on ResetL signal to initiate a module reset
IntL Assert Time	ton_IntL		200	ms	Time from occurrence of condition triggering IntL until Vout:IntL = VOL
IntL Deassert Time	toff_IntL		500	µs	Time from clear on read (**) operation of associated flag until Vout:IntL=VOH. This includes deassert times for Rx LOS, Tx Fault, and other flag bits
Rx LOS Assert Time	ton_los		100	ms	Time from Rx LOS condition present to Rx LOS bit set (value = 1) and IntL asserted
Rx LOS Deassert Time	toff_losf		3	ms	Time from Rx LOS condition absent to negation of Rx LOS status bit
Tx Disable Assert Time	ton_txdis		100	ms	Time from Tx Disable bit set (value = 1) (***) until optical output falls below 10% of nominal
Tx Disable Deassert Time	toff_txdis		400	ms	Time from Tx Disable bit cleared (value = 0) (***) until optical output rises above 90% of nominal
Tx Fault Assert Time	ton_Txfault		200	ms	Time from Tx Fault condition to the Fault bit set (value = 1) and IntL asserted
Alarm and Warning Flag Assert Time	ton_flag		200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value = 1) and IntL asserted
Mask Assert Time	ton_mask		100	ms	Time from mask bit set (value = 1) (***) until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask		100	ms	Time from mask bit cleared (value = 0) (***) until associated IntL operation resumes
Rx Squelch Assert Time	ton_rxsq		15	ms	Time from loss of Rx input signal until squelched output condition is reached
Tx Squelch Assert Time	ton_txsq		400	ms	Time from loss of Tx input signal until squelched output condition is reached
Tx Squelch Deassert Time	toff_txsq		1.5	s	Time from resumption of Tx input signal until normal Tx output condition is reached

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITIONS
Rx Output Disable Assert Time	ton_rxdis		100	ms	Time from Rx Output Disable bit set (value = 1) (***) until Rx output falls below 10% of nominal
Rx Output Disable Deassert Time	toff_rxdis		100	ms	Time from Rx Output Disable bit cleared (value = 0) (***) until Rx output rises above 90% of nominal
Squelch Disable Assert Time	ton_sqdis		100	ms	Time from bit cleared (value = 1) (***) until squelch functionality is disabled. Applies to both Tx and Rx Squelch
Squelch Disable Deassert Time	toff_sqdis		100	ms	Time from bit set (value = 0) (***) until squelch functionality is disabled. Applies to both Tx and Rx Squelch

(*) Power on is defined as the instant when supply voltages reach and remain above the minimum operating value.
(**) Measured from the rising edge of SDA in the stop bit of the read transaction.
(***) Measured from the rising edge of SDA in the stop bit of the write transaction.

FAULT BEHAVIOR

The Tx Fault indicator of the module will trigger (Tx Fault bit set to 1) when any of the Tx high or low output power alarms, Tx loss of lock alarm, or the Tx bias current high or low alarms are triggered. Any of the contributing alarm conditions may be masked per the mask control registers provided in the corresponding module EEPROM/memory registers.

The Rx LOS indicator of the module will assert when the Rx low power alarm asserts and deassert when the Rx low power alarm deasserts. For Rx low power alarm threshold values, see the corresponding module memory map registers.

MONITOR ACCURACY

The module analog monitors have accuracy as defined below.

MONITOR	ACCURACY
RX input power monitor	+/- 3 dB
TX output power monitor	+/- 3 dB
TX bias current monitor	+/- 10%
Case temperature monitor	+/- 3C
Supply voltage monitor	+/- 10%

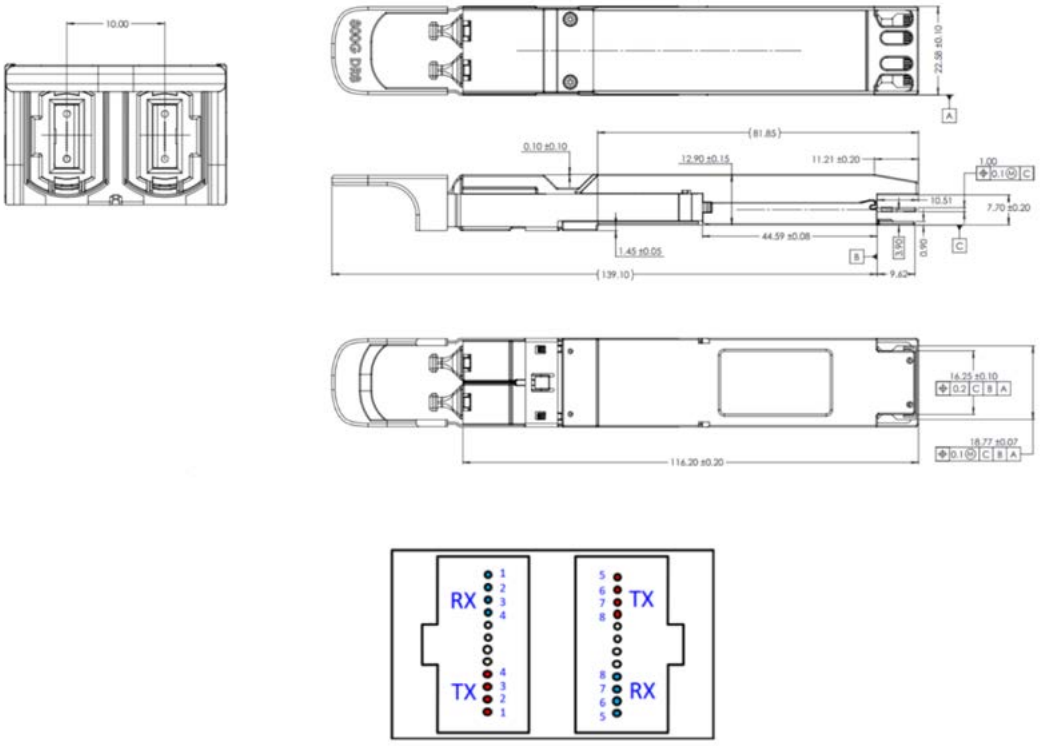
REGISTER MAPPING

The module complies with the OSFP/CMIS memory map specification.

Mechanical Specifications

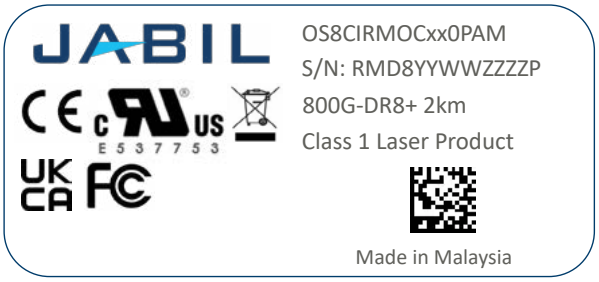
The module housing, mechanical features, and electrical connector are compliant with OSFP mechanical specifications. The module optical connector is two standard MPO-12 duplex receptacle (APC) compliant with IEC-61754 and EIA/TIA-604-18.

MECHANICAL DRAWING



Label Specification

The following printed label is attached to the product (note that the certification labels will be added/removed according to requests and certification process results):



Regulatory and Compliance

EMC — Immunity	• EN 55024 (EU) • IEC EN 61000-4-3 (International)	• EMC Directive 89/336/EEC • IEC /CISPR/24
EMC — Emission	• CISPR 22, class B (Comité International Spécial des Perturbations Radioélectriques--CISPR; Special international committee on radio interference. International). • AS/NZS CISPR22 (Australia/New Zealand)	• VCCI-03 (Japan) • FCC 47 CFR Part 15, class B (US) • ICES-003, Issue 4 (Canada) • EN 55022 (EU) • EMC Directive 2004/108/EEC (EU)
ESD Threshold	• Per MIL-STD 883C Method 3015.4 or ANSI/ESDA/JEDEC JS-001-2012 (component level). • IEC EN 61000-4-2; +/- 8kV contact, +/- 15kV air.	
Product Safety	• UL Recognized Component: UL 60950-1 (2nd Ed.) Information Technology Equipment; CAN/CSA-C22.2 No. 60950-1 (2007) Information Technology Equipment; UL94-V0 flammability. • CB Certificate: IEC 60950-1 (2005 +A1:2009) Information Technology Equipment.	
Fire Safety	• PCB material must be fully compliant to UL796; Temperature class B (IEC 60085); flammability class V-0- UL94). • Cables and connectors must have a flammability ratings of V0- UL94; Service temp.≥90 C. • Label materials must have a flammability ratings of V0- UL94; Service temp.≥90 C. • Optical fibers must have a flammability ratings of V0- UL94; Service temp.≥85 C.	

Optical Safety	• FDA/CDRH certified with accession number, Class 1 laser product:
	  • U.S. 21 CFR 1040;
	  • UL mark
	• UL Certificate:
	  • IEC 60825-1:2014;
	  • EN 60825-1:2014 + A11:2021
		• Complies with 21 CFR 1040.10 and 1040.11 except for conformance with IEC 60825-1 Ed. 3., as described in Laser Notice No. 56, dated May 8, 2019.
		• Caution – Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

RoHS	• 2002/95/EC and the revised and recast Directive 2011/65/EC (RoHS) Restriction on Hazardous Substances. • 2006/1907/EC (REACH) Registration, Evaluation, Authorization of Chemicals.	• JIG 101-A, JIG 101-B Joint Industry Guide Japanese Material Composition Declaration. • CAITEC SJ/T 11363-2006 Requirements for Concentration Limits for Certain Hazardous Substances in Electronic Information Products (China RoHS) • Complies with RoHS II Directive 2011/65/EU.

For additional information, visit jabil.com

Ordering Information

JABIL PART NUMBER	DESCRIPTION	PACKAGE	RATE	REACH
OS8CIRMOCxx0PAM	800 Gb/s DR8+ OSFP Optical Transceiver with Dual MPO-12 Optical Connector, 2km Reach	OSFP	850Gb/s	2km
OS8CS3MOCxx0PAM	800 Gb/s DR8 OSFP Optical Transceiver with Dual MPO-12 Optical Connector, 500m Reach	OSFP	850Gb/s	500m

Document Version

VERSION	DATE	NOTES
1.0	11/21/2023	Initial specification version
1.1	7/8/2024	Updated Regulatory and Compliance

Manufacturer's Address

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