800G Active Optical Cable

Jabil Photonic 800G Active Optical Cable provides optimized solutions for interconnections inside datacenter at 800Gb/s up to 50m. Product is available in OSFP form to satisfy the different host system requirements. Transmission is based on VCSEL 850nm with electrical driver, while Receiver side is based on PIN photodetector and TIA. Module is equipped with DSP to provide channel equalization, PAM4 retimer and supports electrical lanes loss on host system with up to 30dB.

FEATURES

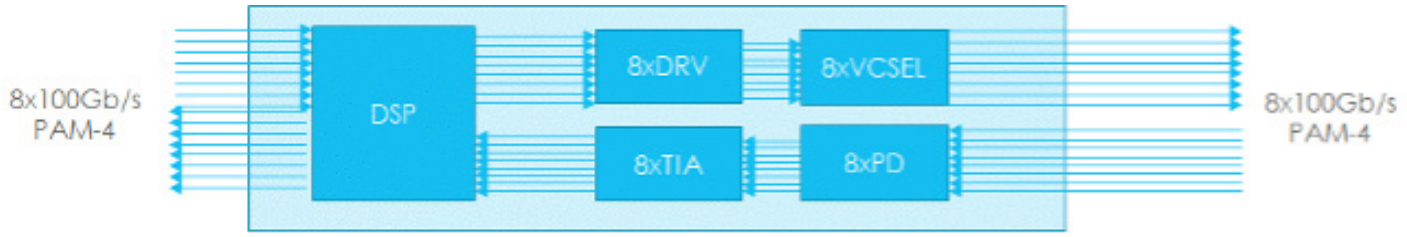
- 800G OSFP form factor options
- 8x106.25Gb/s transmission each lane
- Host side up to 30dB of electrical loss
- DSP for equalization and performance
- Cable length: 3m, 10m, 50m
- Operating temperature 0° to 70°C
- CMIS 5.0 standard interface

APPLICATIONS

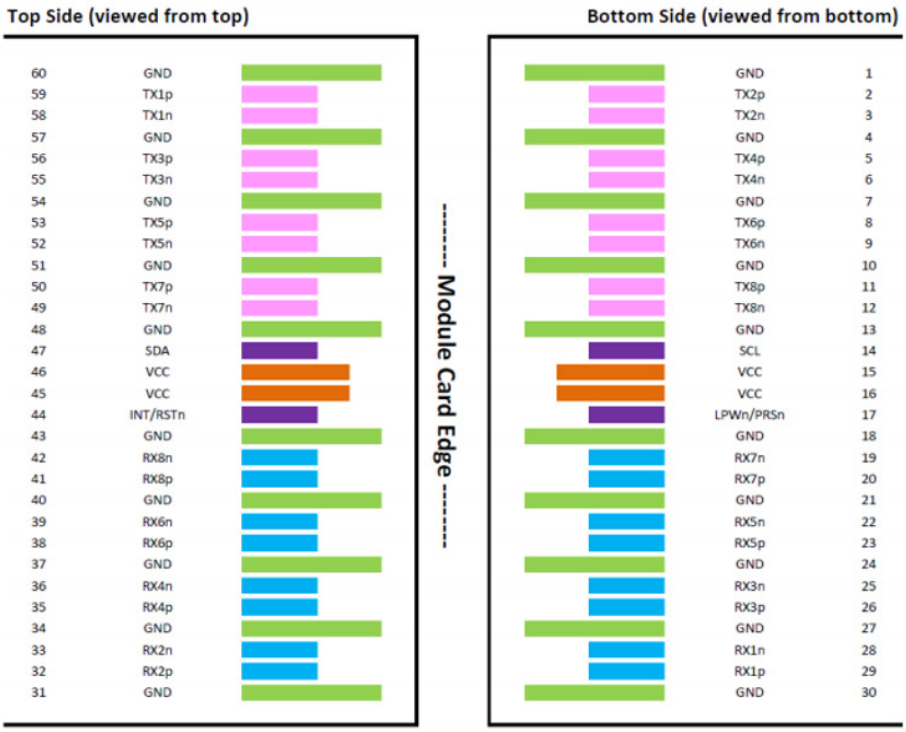
- Intra-datacenter short connections

For additional information, visit jabil.com

PRODUCT ARCHITECTURE



OSFP PIN DIAGRAM



PIN DESCRIPTIONS

NAME	DIRECTION	DESCRIPTION
TX[8:1]p	input	Transmit differential pairs non-inverted from host to module.
TX[8:1]n	input	Transmit differential pairs inverted from host to module.
RX[8:1]p	output	Receive differential pairs non-inverted from module to host.
RX[8:1]n	output	Receive differential pairs inverted from module to host.
SCL	bidir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host.
SDA	bidir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.
PWn/PRSn	bidir	Multi-level signal for low power control from host to module and module presence indication from module to host.
INT/RSTn	bidir	Multi-level signal for interrupt request from module to host and reset control from host to module.
VCC	power	3.3V power for module.
GND	ground	Module Ground. Logic and power return path.

PIN LIST

PIN#	SYMBOL	DESCRIPTION	LOGIC	DIRECTION	PLUG SEQUENCE[2]	NOTES
1	GND	Ground			1	
2	TX2p	TX Non-Inverted	CML-I	Input from Host	3	
3	TX2n	TX Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	TX Non-Inverted	CML-I	Input from Host	3	
6	TX4n	TX Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	TX Non-Inverted	CML-I	Input from Host	3	
9	TX6n	TX Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	TX Non-Inverted	CML-I	Input from Host	3	
12	TX8n	TX Inverted	CML-I	Input from Host	3	

(1) Open-Drain with pull up resistor on Host.

(2) Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1, 2, 3

PIN#	SYMBOL	DESCRIPTION	LOGIC	DIRECTION	PLUG SEQUENCE[2]	NOTES
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3	1
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/ PRSn	Low-Power Mode/ Module Present	Multi-Level	Bi-directional	3	
18	GND	Ground			1	
19	RX7n	RX Inverted	CML-O	Output to Host	3	
20	RX7p	RX Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	RX Inverted	CML-O	Output to Host	3	
23	RX5p	RX Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	RX Inverted	CML-O	Output to Host	3	
26	RX3p	RX Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	RX Inverted	CML-O	Output to Host	3	
29	RX1p	RX Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	
31	GND	Ground			1	
32	RX2p	RX Non-Inverted	CML-O	Output to Host	3	
33	RX2n	RX Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	RX Non-Inverted	CML-O	Output to Host	3	
36	RX4n	RX Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	RX Non-Inverted	CML-O	Output to Host	3	
39	RX6n	RX Inverted	CML-O	Output to Host	3	

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PIN#	SYMBOL	DESCRIPTION	LOGIC	DIRECTION	PLUG SEQUENCE[2]	NOTES
40	GND	Ground			1	
41	RX8p	RX Non-Inverted	CML-O	Output to Host	3	
42	RX8n	RX Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt/Module Reset	Multi-Level	Bi-directional	3	
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3	1
48	GND	Ground			1	
49	TX7n	TX Inverted	CML-I	Input from Host	3	
50	TX7p	TX Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	TX Inverted	CML-I	Input from Host	3	
53	TX5p	TX Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	TX Inverted	CML-I	Input from Host	3	
56	TX3p	TX Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	TX Inverted	CML-I	Input from Host	3	
59	TX1p	TX Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

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ABSOLUTE MAXIMUM RATINGS

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

PARAMETER	SYMBOL	MIN	TYPICAL	MAX	UNIT	NOTES
Storage Temperature	T_S	-40		85	ºC	
Storage Ambient Humidity	H_A	0		85	%	
Maximum Supply Voltage	V_{CC}	-0.5		3.6	V	

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYPICAL	MAX	UNIT	NOTES
Operating Case Temperature	Tcase	0	25	70	ºC	
Supply Voltage	VCC	3.135	3.3	3.465	V	
Relative Humidity	RH	5		85	%	
Data Rate (Optical)	DRO		8x106.25		Gbps	
Data Rate (Electrical)	DRE		8x106.25		Gbps	

ELECTRICAL CHARACTERISTICS

800G to 800G AOC Operation (EOL, Tcase= 5~65º, VCC=3.135~3.465 V)

PARAMETER	SYMBOL	MIN	TYPICAL	MAX	UNIT	NOTES
Power Dissipation	P_d		15	16	W	Each end
TRANSMITTER						
Data Rate, each lane	DRE		106.25		Gbps	
Differential Voltage pk-pk	VIN	40		900	mV	
Input differential impedance	ZIN		100		Ohm	
Differential Termination Resistance Mismatch				10	%	
RECEIVER						
Data Rate, each lane	DRE		106.25		Gbps	
Output differential impedance	Z_{OUT}		100		Ohm	
Differential Termination Resistance Mismatch				10	%	
Differential output voltage	V_{OUT}			1000	mV	

OPTICAL CHARACTERISTICS

800G to 800G AOC Operation (EOL, Tcase= 5~65°, VCC=3.135~3.465 V)

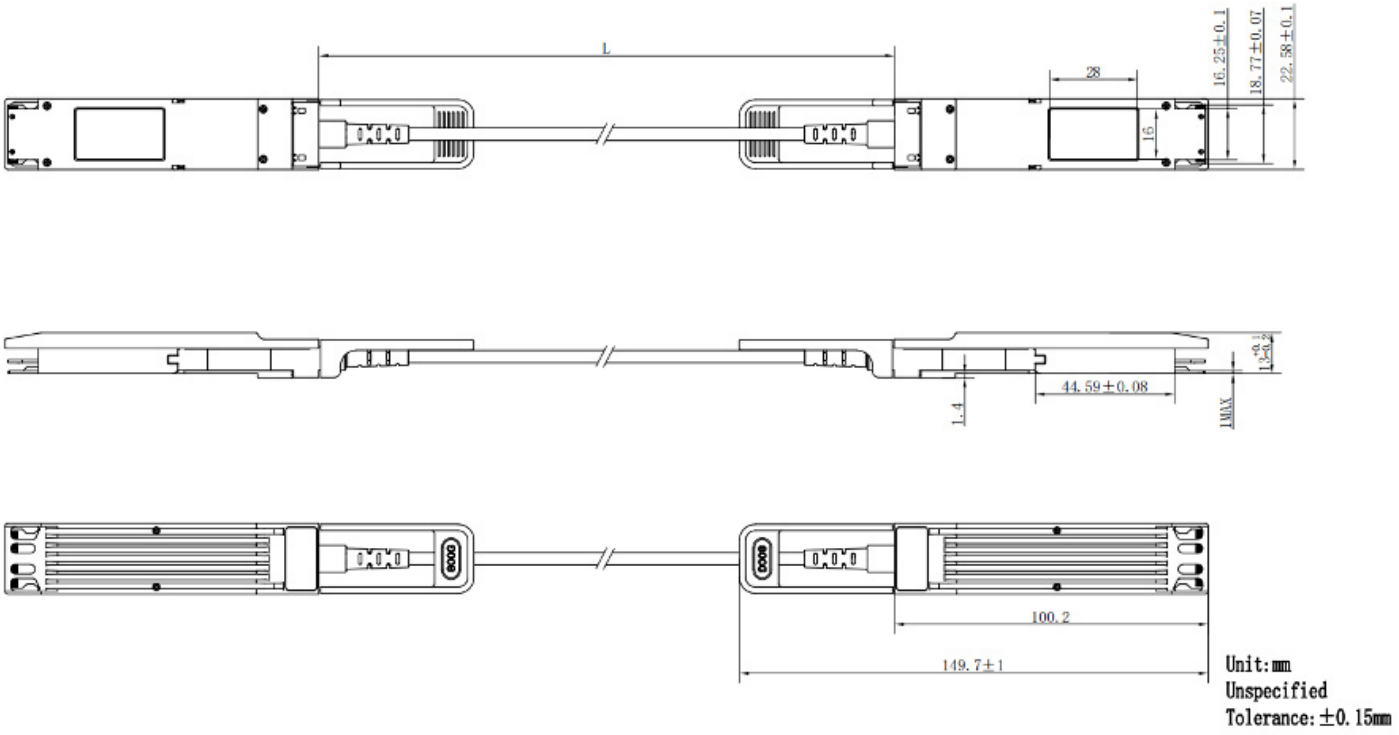
PARAMETER	SYMBOL	MIN	TYPICAL	MAX	UNIT	NOTES
Signaling Speed per Lane	DRO		106.25		Gbps	
Center Wavelength	λ		850		nm	
RMS Spectral Width	Δλ			0.6	nm	
Average launch power		-1		4	dBm	
TX TDECQ				4.4	dB	
TX ER		2.5			dB	

ORDERING INFORMATION

JABIL PART NUMBER	PACKAGE	RATE	REACH	OTHER INFO
OS8CXXACC00Y000	OSFP-finned & flat top	800G	XX=fiber length	C-temp AOC Y=F in case of finned top, Y=0 in case of flat top

Note: additional cable lengths can be provided on request.

MECHANICAL SPECIFICATIONS



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REGULATORY COMPLIANCE

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FEATURE	REFERENCE STANDARDS	PERFORMANCE
ESD-HBM	JESD22-A114-B	1KV high speed Pins, 2KV other Pins
ESD-Air Discharge	IEC 61000-4-2	+/-15KV
ESD-Contact Discharge	IEC 61000-4-2	+/-8KV
EMC-RE	FCC Part 15 Class B	
EMC-RS	IEC 61000 4-3	
ROHS 2.0	2011/65/EU	

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