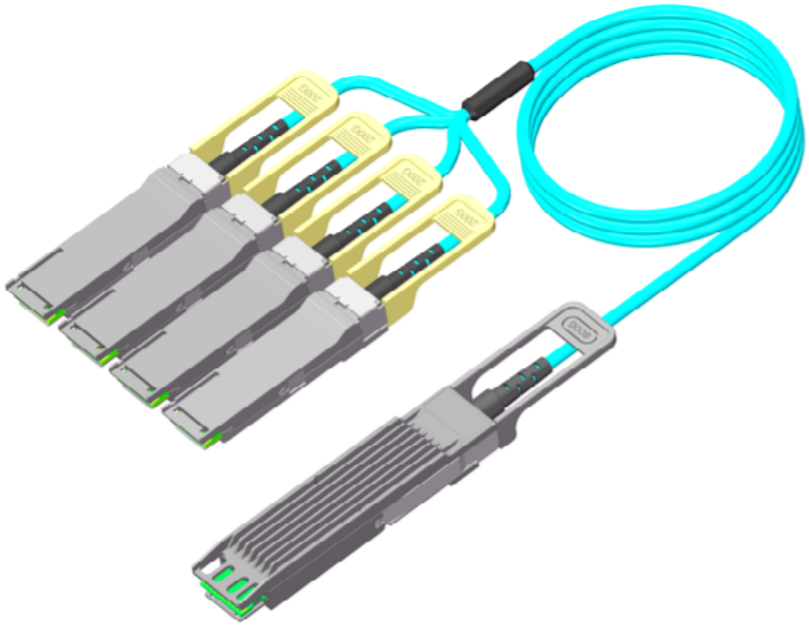
# 800G Active Optical Cable
## (Breakout Cable 4x200G)

Jabil Photonic 800G Active Optical Cable (breakout 4x200G) provides optimized solutions for interconnections inside datacenter up to 50M on OM4 fiber. Products is in OSFP form on the 800G side and is in QSFP112 form on the 200G side to satisfy the different host system requirements. Transmission is based on VCSEL 850nm with electrical driver, while Receiver side is based on PIN photodetector and TIA. Module is equipped with DSP to provide channel equalization, PAM4 retimer and supports electrical lanes loss on host system with up to 30dB.

### FEATURES

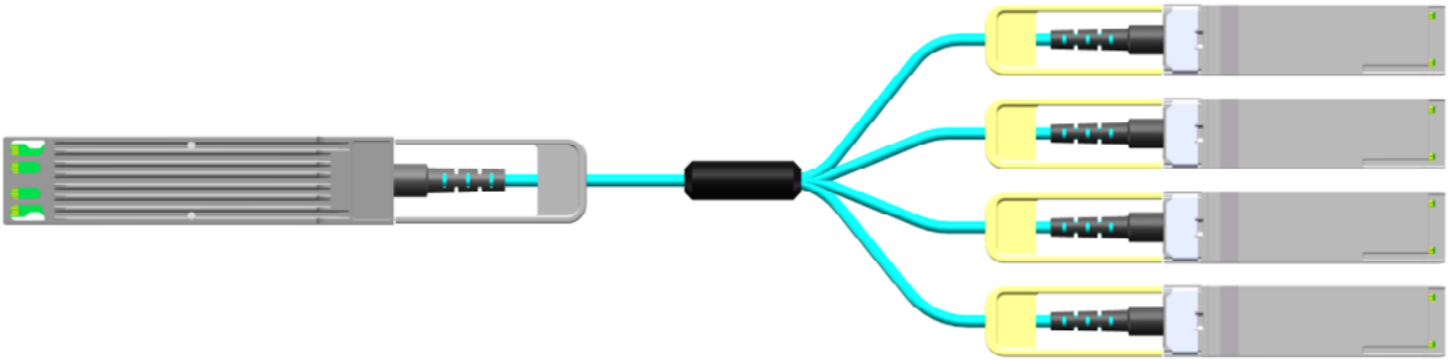
- OSFP and QSFP112 MSA compliant
- 106.25Gb/s transmission for each direction
- Host side up to 30dB of electrical loss
- DSP for equalization and performance
- Cable length: 3m, 10m, 50m
- Operating temperature 0° to 70°C
- CMIS 5.0 standard interface



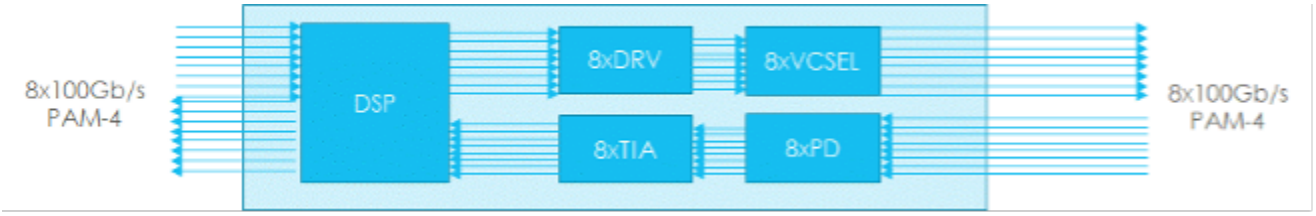
### APPLICATIONS

- Intra-datacenter short connections

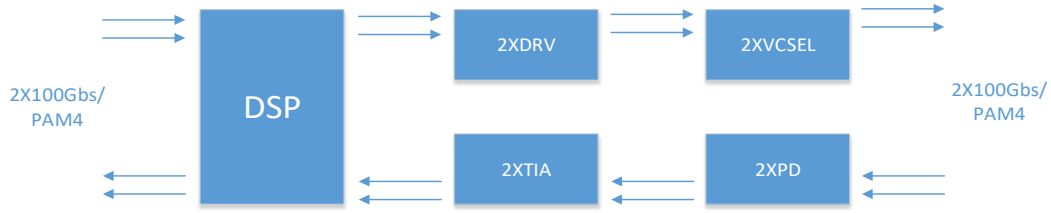
## PRODUCT ARCHITECTURE



## 800G END




## 200G END (CHANNEL 1/2 ARE USED)

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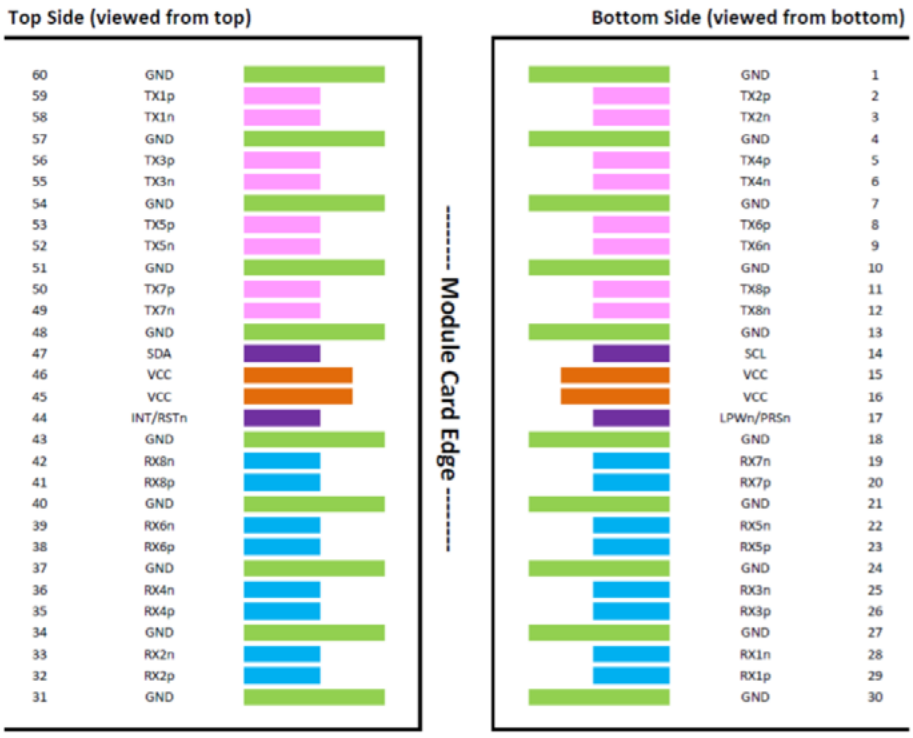
## OSFP PIN DIAGRAM




## OSFP PIN DESCRIPTIONS

| PIN# | SYMBOL | DESCRIPTION | LOGIC | DIRECTION | PLUG SEQUENCE[2] | NOTES |
|---|---|---|---|---|---|---|
| 1 | GND | Ground | | | 1 | |
| 2 | TX2p | TX Non-Inverted | CML-I | Input from Host | 3 | |
| 3 | TX2n | TX Inverted | CML-I | Input from Host | 3 | |
| 4 | GND | Ground | | | 1 | |
| 5 | TX4p | TX Non-Inverted | CML-I | Input from Host | 3 | |
| 6 | TX4n | TX Inverted | CML-I | Input from Host | 3 | |
| 7 | GND | Ground | | | 1 | |
| 8 | TX6p | TX Non-Inverted | CML-I | Input from Host | 3 | |
| 9 | TX6n | TX Inverted | CML-I | Input from Host | 3 | |
| 10 | GND | Ground | | | 1 | |

(1) Open-Drain with pull up resistor on Host.

(2) Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1, 2, 3

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| PIN# | SYMBOL | DESCRIPTION | LOGIC | DIRECTION | PLUG SEQUENCE[2] | NOTES |
|---|---|---|---|---|---|---|
| 11 | TX8p | TX Non-Inverted | CML-I | Input from Host | 3 | |
| 12 | TX8n | TX Inverted | CML-I | Input from Host | 3 | |
| 13 | GND | Ground | | | 1 | |
| 14 | SCL | 2-wire Serial interface clock | LVCMOS-I/O | Bi-directional | 3 | 1 |
| 15 | VCC | +3.3V Power | | Power from Host | 2 | |
| 16 | VCC | +3.3V Power | | Power from Host | 2 | |
| 17 | LPWn/ PRSn | Low-Power Mode/ Module Present | Multi-Level | Bi-directional | 3 | |
| 18 | GND | Ground | | | 1 | |
| 19 | RX7n | RX Inverted | CML-O | Output to Host | 3 | |
| 20 | RX7p | RX Non-Inverted | CML-O | Output to Host | 3 | |
| 21 | GND | Ground | | | 1 | |
| 22 | RX5n | RX Inverted | CML-O | Output to Host | 3 | |
| 23 | RX5p | RX Non-Inverted | CML-O | Output to Host | 3 | |
| 24 | GND | Ground | | | 1 | |
| 25 | RX3n | RX Inverted | CML-O | Output to Host | 3 | |
| 26 | RX3p | RX Non-Inverted | CML-O | Output to Host | 3 | |
| 27 | GND | Ground | | | 1 | |
| 28 | RX1n | RX Inverted | CML-O | Output to Host | 3 | |
| 29 | RX1p | RX Non-Inverted | CML-O | Output to Host | 3 | |
| 30 | GND | Ground | | | 1 | |
| 31 | GND | Ground | | | 1 | |
| 32 | RX2p | RX Non-Inverted | CML-O | Output to Host | 3 | |
| 33 | RX2n | RX Inverted | CML-O | Output to Host | 3 | |
| 34 | GND | Ground | | | 1 | |
| 35 | RX4p | RX Non-Inverted | CML-O | Output to Host | 3 | |
| 36 | RX4n | RX Inverted | CML-O | Output to Host | 3 | |
| 37 | GND | Ground | | | 1 | |

(1) Open-Drain with pull up resistor on Host.

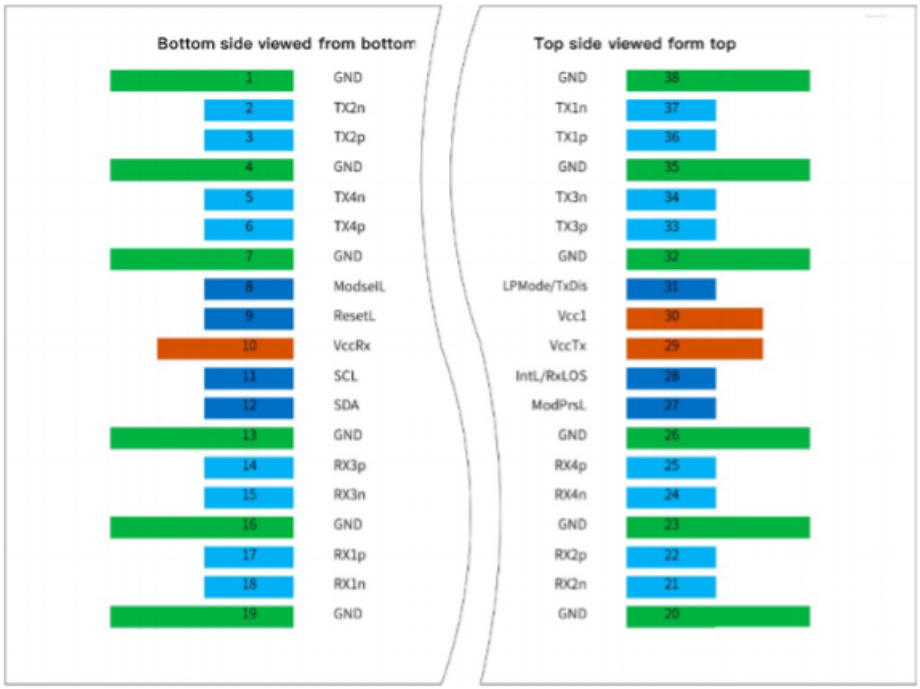
(2) Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1, 2, 3

| PIN# | SYMBOL | DESCRIPTION | LOGIC | DIRECTION | PLUG SEQUENCE[2] | NOTES |
|---|---|---|---|---|---|---|
| 38 | RX6p | RX Non-Inverted | CML-O | Output to Host | 3 | |
| 39 | RX6n | RX Inverted | CML-O | Output to Host | 3 | |
| 40 | GND | Ground | | | 1 | |
| 41 | RX8p | RX Non-Inverted | CML-O | Output to Host | 3 | |
| 42 | RX8n | RX Inverted | CML-O | Output to Host | 3 | |
| 43 | GND | Ground | | | 1 | |
| 44 | INT/RSTn | Module Interrupt/Module Reset | Multi-Level | Bi-directional | 3 | |
| 45 | VCC | +3.3V Power | | Power from Host | 2 | |
| 46 | VCC | +3.3V Power | | Power from Host | 2 | |
| 47 | SDA | 2-wire Serial interface data | LVCMOS-I/O | Bi-directional | 3 | 1 |
| 48 | GND | Ground | | | 1 | |
| 49 | TX7n | TX Inverted | CML-I | Input from Host | 3 | |
| 50 | TX7p | TX Non-Inverted | CML-I | Input from Host | 3 | |
| 51 | GND | Ground | | | 1 | |
| 52 | TX5n | TX Inverted | CML-I | Input from Host | 3 | |
| 53 | TX5p | TX Non-Inverted | CML-I | Input from Host | 3 | |
| 54 | GND | Ground | | | 1 | |
| 55 | TX3n | TX Inverted | CML-I | Input from Host | 3 | |
| 56 | TX3p | TX Non-Inverted | CML-I | Input from Host | 3 | |
| 57 | GND | Ground | | | 1 | |
| 58 | TX1n | TX Inverted | CML-I | Input from Host | 3 | |
| 59 | TX1p | TX Non-Inverted | CML-I | Input from Host | 3 | |
| 60 | GND | Ground | | | 1 | |

(1) Open-Drain with pull up resistor on Host.

(2) Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1, 2, 3

## QSFP112 PIN DIAGRAM




## QSFP112 PIN DESCRIPTIONS

| PAD | LOGIC | SYMBOL | DESCRIPTION | PLUG SEQUENCE | NOTES |
|---|---|---|---|---|---|
| 1 | | GND | Ground | 1 | 1 |
| 2 | CML-I | Tx2n | Transmitter Inverted Data Input | 3 | |
| 3 | CML-I | Tx2p | Transmitter Non-Inverted Data Input | 3 | |
| 4 | | GND | Ground | 1 | 1 |
| 5 | CML-I | Tx4n | Transmitter Inverted Data Input | 3 | 3 |
| 6 | CML-I | Tx4p | Transmitter Non-Inverted Data Input | 3 | 3 |
| 7 | | GND | Ground | 1 | 1 |
| 8 | LVTTL-I | ModSelL | Select | 3 | |
| 9 | LVTTL-I | ResetL | Reset | 3 | |
| 10 | | Vcc Rx | +3.3 V Power supply receiver | 2 | 2 |

(1) GND is the symbol for signal and supply (power) common for the QSFP112 module. All are common within the QSFP112 module and all voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

(2) Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently.

(3) Not defined on the 200G end.

| PAD | LOGIC | SYMBOL | DESCRIPTION | PLUG SEQUENCE | NOTES |
|---|---|---|---|---|---|
| 11 | LVCMOS-I/O | SCL | 2-wire serial interface clock | 3 | |
| 12 | LVCMOS-I/O | SDA | 2-wire serial interface data | 3 | |
| 13 | | GND | Ground | 1 | 1 |
| 14 | CML-O | Rx3p | Receiver Non-Inverted Data Output | 3 | 3 |
| 15 | CML-O | Rx3n | Receiver Inverted Data Output | 3 | 3 |
| 16 | | GND | Ground | 1 | 1 |
| 17 | CML-O | Rx1p | Receiver Non-Inverted Data Output | 3 | |
| 18 | CML-O | Rx1n | Receiver Inverted Data Output | 3 | |
| 19 | | GND | Ground | 1 | 1 |
| 20 | | GND | Ground | 1 | 1 |
| 21 | CML-O | Rx2n | Receiver Inverted Data Output | 3 | |
| 22 | CML-O | Rx2p | Receiver Non-Inverted Data Output | 3 | |
| 23 | | GND | Ground | 1 | 1 |
| 24 | CML-O | Rx4n | Receiver Inverted Data Output | 3 | 3 |
| 25 | CML-O | Rx4p | Receiver Non-Inverted Data Output | 3 | 3 |
| 26 | | GND | Ground | 1 | 1 |
| 27 | LVTTL-O | ModPrsL | Present | 3 | |
| 28 | LVTTL-O | IntL/RxLOS | Interrupt/optional RxLOS | 3 | |
| 29 | | Vcc Tx | +3.3 V Power supply transmitter | 2 | 2 |
| 30 | | Vcc1 | +3.3 V Power Supply | 2 | 2 |
| 31 | LVTTL-I | LPMode/ Tx Dis | Low Power Mode/optional TX Disable | 3 | |
| 32 | | GND | Ground | 1 | 1 |
| 33 | CML-I | Tx3p | Transmitter Non-Inverted Data Input | 3 | 3 |
| 34 | CML-I | Tx3n | Transmitter Inverted Data Input | 3 | 3 |
| 35 | | GND | Ground | 1 | 1 |
| 36 | CML-I | Tx1p | Transmitter Non-Inverted Data Input | 3 | |
| 37 | CML-I | Tx1n | Transmitter Inverted Data Input | 3 | |
| 38 | | GND | Ground | 1 | |

(1) GND is the symbol for signal and supply (power) common for the QSFP112 module. All are common within the QSFP112 module and all voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

(2) Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently.

(3) Not defined on the 200G end.

## ABSOLUTE MAXIMUM RATINGS

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

| PARAMETER | SYMBOL | MIN | TYPICAL | MAX | UNIT | NOTES |
|---|---|---|---|---|---|---|
| Storage Temperature | $T_S$ | -40 | | 85 | ºC | |
| Storage Ambient Humidity | $H_A$ | 0 | | 85 | % | |
| Maximum Supply Voltage | $V_{CC}$ | -0.5 | | 3.6 | V | |

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN | TYPICAL | MAX | UNIT | NOTES |
|---|---|---|---|---|---|---|
| Operating Case Temperature | Tcase | 0 | 25 | 70 | ºC | |
| Supply Voltage | VCC | 3.135 | 3.3 | 3.465 | V | |
| Relative Humidity | RH | 5 | | 85 | % | |
| Data Rate (Optical) | DRO | | 8x106.25 | | Gbps | 800G end |
| | | | 2x106.25 | | Gbps | 200G end |
| Data Rate (Electrical) | DRE | | 8x106.25 | | Gbps | 800G end |
| | | | 2x106.25 | | Gbps | 200G end |

## ELECTRICAL CHARACTERISTICS

| PARAMETER | SYMBOL | MIN | TYPICAL | MAX | UNIT | NOTES |
|---|---|---|---|---|---|---|
| Power Dissipation | $P_d$ | | | 16 | W | 800G end |
| | | | | 4 | W | 200G end |
| TRANSMITTER | | | | | | |
| Data Rate, each lane | DRE | | 106.25 | | Gbps | |
| Differential Voltage pk-pk | VIN | 40 | | 900 | mV | |
| Input differential impedance | ZIN | | 100 | | Ohm | |
| Differential Termination Resistance Mismatch | | | | 10 | % | |
| RECEIVER | | | | | | |
| Data Rate, each lane | DRE | | 106.25 | | Gbps | |
| Output differential impedance | $Z_{OUT}$ | | 100 | | Ohm | |
| Differential Termination Resistance Mismatch | | | | 10 | % | |
| Differential output voltage | $V_{OUT}$ | | | 1000 | mV | |

## OPTICAL CHARACTERISTICS

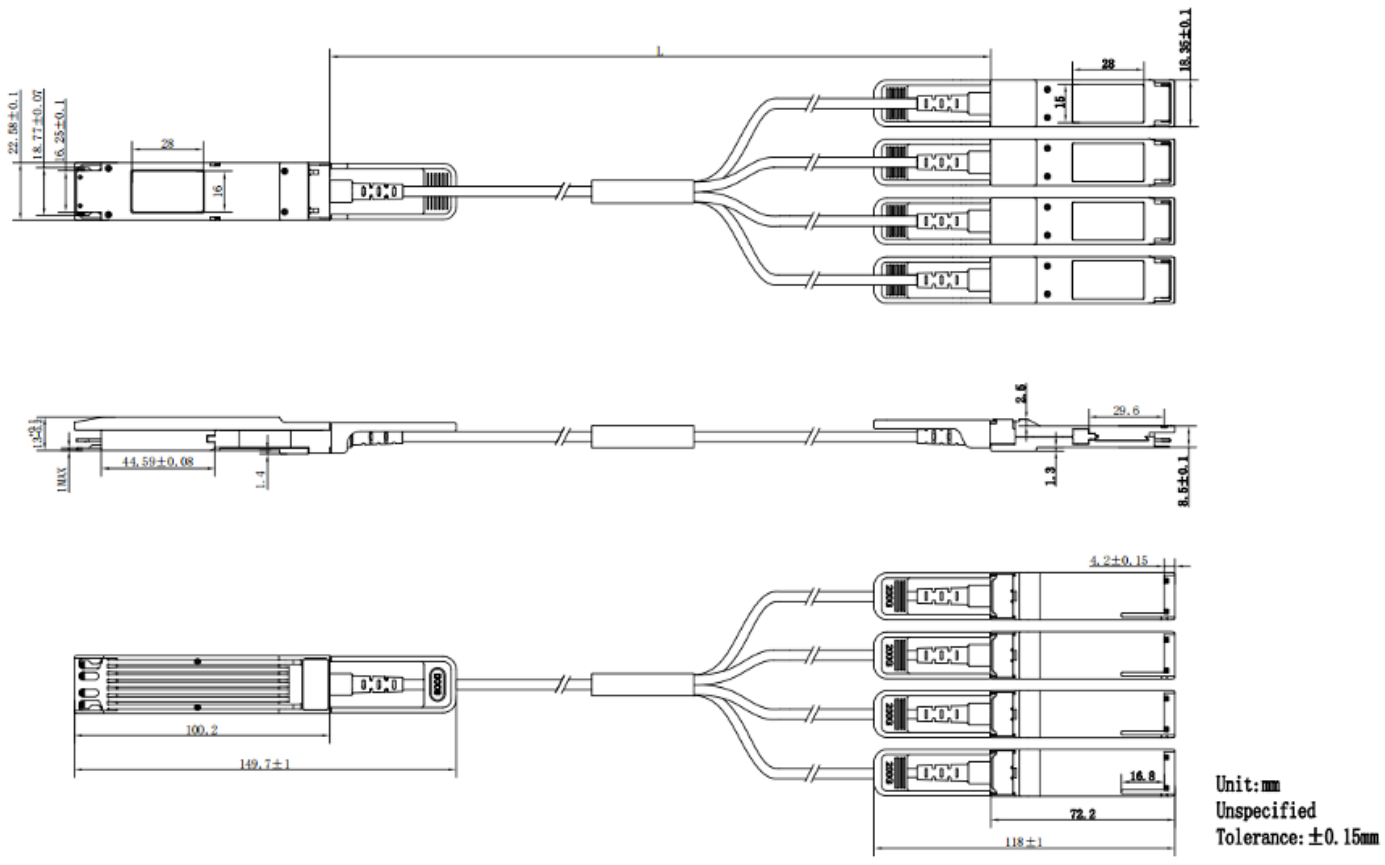
| PARAMETER | SYMBOL | MIN | TYPICAL | MAX | UNIT | NOTES |
|---|---|---|---|---|---|---|
| Signaling Speed per Lane | DRO | | 106.25 | | Gbps | |
| Center Wavelength | λ | | 850 | | nm | |
| RMS Spectral Width | Δλ | | | 0.6 | nm | |
| Average launch power | | -1 | | 4 | dBm | |
| TX TDECQ | | | | 4.4 | dB | |
| TX ER | | 2.5 | | | dB | |

## ORDERING INFORMATION

| JABIL PART NUMBER | PACKAGE | REACH | OTHER INFO |
|---|---|---|---|
| OS8CXXACC00Y4ZZ | 800G OSFP to 4x200G BREAKOUT | XX=fiber length | C-temp AOC |

Note: additional cable lengths can be provided on request.

## AOC MECHANICAL SPECIFICATIONS



## REGULATORY COMPLIANCE

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

| FEATURE | REFERENCE STANDARDS | PERFORMANCE |
|---|---|---|
| ESD-HBM | JESD22-A114-B | 1KV high speed Pins, 2KV other Pins |
| ESD-Air Discharge | IEC 61000-4-2 | +/-15KV |
| ESD-Contact Discharge | IEC 61000-4-2 | +/-8KV |
| EMC-RE | FCC Part 15 Class B | |
| EMC-RS | IEC 61000 4-3 | |
| ROHS 2.0 | 2011/65/EU | |

For additional information, visit jabil.com

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