400G QSFP-DD FR4/LR4 Optical Transceiver

Jabil 400 Gb/s FR4/LR4 QSFP-DD Optical Transceiver is a small form-factor, high speed, and low power consumption product targeted for use in optical interconnects for data communications applications. The high bandwidth module supports 400G Ethernet connections via LC connector over parallel single-mode fiber links up to 2 km and 10 km for the FR4 and LR4 variants.

FEATURES

- Compliant with 4x 100G Lambda MSA 100G-FR/-LR and IEEE 802.3cu 400GBASE-FR4/-LR4
- Electrical interface compliant with IEEE 802.3bs 400GAUI-8 (CDAUI-8) standard
- Compact Type 2 QSFP-DD form factor for high faceplate density in networking equipment and cage backward compatibility with QSFP28
- Compatibility with single-mode optical connectors and cable infrastructures
- Operating temperature range: 0° to 70°C
- CMIS-compliant management interface with full module diagnostics and control through I2C
- Single 3.3V Power supply
- Power consumption < 10W
- RoHS-6 Compliance

APPLICATIONS

- 400GbE connectivity for large-scale cloud and enterprise data centers
- Ethernet switch, router, and client-side telecom interfaces

STANDARDS

- QSFP-DD MSA
- IEEE 802.3cu
- IEEE 802.3bs
- 100G Lambda MSA

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Storage Temperature	Ts	-40	+85	ºC
Case Operating Temperature	Tc	0	70	ºC
Relative Humidity (*)	RH	5	85	%
DC Supply Voltage	V_{CC}	-	3.6	V
ESD (HBM)	V_{ESD}	-1k	1k	V
Differential Input Voltage	$V_{in\text{-}pp}$	-	1600	mVpp
Receiver Input Optical Power	P_{IN} (max)	-	+3.5	dBm

(*) not condensing

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Operating Case Temperature	TCASE	0	30	70	°C
DC Supply Voltage	V_{CC}	3.135	3.3	3.465	V
Power Supply Noise Tolerance (*)		-	-	50	mVpp
Bit Rate	BR	53.12	53.125	53.13	Gbps

(*) At input to recommended power supply filter

Optical Transmitter

The 400G FR4 optical transceiver electrical interface is compliant to the IEEE 802.3bs 400GAUI-8 (CDAUI-8) host to module retimed interface (see IEEE 802.3bs Annex 120E). The 400G FR4/LR4 optical transmitter is compliant with the IEEE 802.3bs 400GBASE-FR4/-LR4 specification, with four optical lanes of 100G PAM4 data over one single fiber pair of up to 2 km and 10 km, respectively. Each optical lane is compliant with the 100G Lambda MSA 100G-FR/-LR optical interface specification. The FR4/LR4 optical interface standard is defined assuming IEEE standard 400G KP4 RS(544,514) forward error correction (FEC) is implemented in the host or switch equipment in order to enable error-free link operation.

TRANSMITTER ELECTRICAL INPUT CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Data modulation type		PAM4			
Data rate, each lane	BR	53.12	53.125	53.13	Gbps
Baud/symbol rate, each lane	BR	26.56	26.5625	26.565	Gbd
DC common mode voltage	V_{in_CM}	-350	-	2850	mV
Differential input return loss	SDD11	Per IEEE802.3bm Annex 83E, Equation 83E-5			
Differential to common mode input return loss	SDD11	Per IEEE802.3bm Annex 83E, Equation 83E-6			
Differential termination mismatch		-	-	10	%
Module stressed input test		Meets electrical interface pre-FEC BER of $< 10^{-5}$ with stressed input per IEEE802.3bs Annex 120E, section 120E.3.4.1			mV
Single-ended voltage tolerance	V_{in_SE}	-0.4	-	3.3	V

TRANSMITTER OPTICAL OUTPUT CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data modulation type			PAM4			
Data rate, each lane	BR	106.24	106.25	106.26	Gbps	
Baud/symbol rate, each lane	BR	53.12	53.125	53.13	Gbd	
Lane wavelength range		1264.5 to 1277.5 1271 center wavelength			nm	
		1284.5 to 1297.5 1291 center wavelength				
		1304.5 to 1317.5 1311 center wavelength				
		1324.5 to 1337.5 1331 center wavelength				
Side mode suppression ratio	SMSR	30	-	-	dB	
Average optical output power of OFF transmitter, each lane		-	-	-30	dBm	
Transmitter reflectance		-	-	-26	dB	1
$RIN_{17.1}OMA$	RIN	-	-	-136	dB/Hz	
Optical return loss tolerance	ORLT	-	-	17.1	dB	
Extinction ratio	ER	3.5	-	-	dB	
400G FR4 (2KM PRODUCT VARIANT)						
Average optical output power, each lane	P_{ave}	-3.3	-	3.5	dBm	
Optical modulation amplitude, each lane	OMA_{outer}	-0.3	-	3.7	dBm	
Transmitter dispersion and eye closure penalty, each lane	TDECQ	-	-	3.4	dB	
OMA minus TDECQ, each lane		-1.6	-	-	dBm	
Operating link reach		2	-	2000	m	

TRANSMITTER OPTICAL OUTPUT CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
400G LR4 (10KM PRODUCT VARIANT)						
Average optical output power, each lane	P_{ave}	-2.7	-	5.1	dBm	
Optical modulation amplitude, each lane	OMA_{outer}	-0.3	-	4.4	dBm	
Transmitter dispersion and eye closure penalty, each lane	TDECQ	-	-	3.9	dB	
OMA minus TDECQ, each lane		0.3 for ER <4.5, 0.2 for ER > 4.5	-	4.4	dBm	
Operating link reach		2	-	10000	m	

(1) Transmitter reflectance is defined looking into the transmitter

Optical Receiver

The 400G FR4/LR4 optical transceiver electrical interface is compliant to the IEEE 802.3bs 400GAUI-8 (CDAUI-8) host to module retimed interface (see IEEE 802.3bs Annex 120E). The FR4/LR4 optical interface is defined assuming IEEE standard 400G KP4 RS(544,514) forward error correction (FEC) is implemented in the host or switch equipment, in order to enable error-free link operation.

RECEIVER ELECTRICAL OUTPUT CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Data modulation type			PAM4		
Data rate, each lane	BR	53.12	53.125	53.13	Gbps
Baud/symbol rate, each lane	BR	26.56	26.5625	26.565	Gbd
DC common mode voltage	$V_{out\_AC\text{-}CM}$	-350	-	2850	mV
AC common mode voltage (rms)	$V_{out\_DC\text{-}CM}$	-	-	17.5	mV_{rms}
Differential peak-to-peak output voltage	V_{out_pp}	-	-	900	mV_{pp}
Near-end ESMW (eye symmetry mask width)	$ESMW_{near}$		0.265		UI
Near-end eye height, differential	EH_{near}	70	-	-	mV
Far-end ESMW (eye symmetry mask width)	$ESMW_{far}$		0.2		UI
Far-end eye height, differential	EH_{far}	30	-	-	mV
Far-end pre-cursor ISI ratio		-4.5	-	2.5	%
Differential output return loss	SDD22	Per IEEE802.3bm Annex 83E, Equation 83E-2			
Common to differential mode conversion return loss	SCD22	Per IEEE802.3bm Annex 83E, Equation 83E-3			
Differential termination mismatch		-	-	10	%
Transition time (20-80%)	T_{rf}	9.5	-	-	ps

RECEIVER OPTICAL INPUT CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data modulation type			PAM4			
Data rate, each lane	BR	106.24	106.25	106.26	Gbps	
Baud/symbol rate, each lane	BR	53.12	53.125	53.13	Gbd	
Lane wavelengths		1264.5 to 1277.5 1271 center wavelength			nm	
		1284.5 to 1297.5 1291 center wavelength				
		1304.5 to 1317.5 1311 center wavelength				
		1324.5 to 1337.5 1331 center wavelength				
400G FR4 (2KM PRODUCT VARIANT)						
Average receive power, each lane		-7.3	-	3.5	dBm	
Receive power in OMA_{outer}, each lane		-	-	3.7	dBm	
Damage threshold, each lane		-	-	6.1	dBm	1
Receiver reflectance		-	-	-26	dB	
Unstressed receiver sensitivity (OMA_{outer}), each lane at pre-FEC BER of 2 x 10^{-4}	URS	max(-4.6, SECQ - 6.0),where 0.9 < SECQ < 3.4 dB (PRBS31Q)			dBM	2
Stressed receiver sensitivity (OMA_{outer}), each lane at pre-FEC BER of 2 x 10^{-4}	SRS	-	-	-2.6	dBM	
CONDITIONS OF STRESSED RECEIVER SENSITIVITY TEST						
Stressed eye closure for PAM4 (SECQ), each lane	SECQ		3.4		dB	3
OMA_{outer} of each aggressor lane			1.5		dBm	3

RECEIVER OPTICAL INPUT CHARACTERISTICS

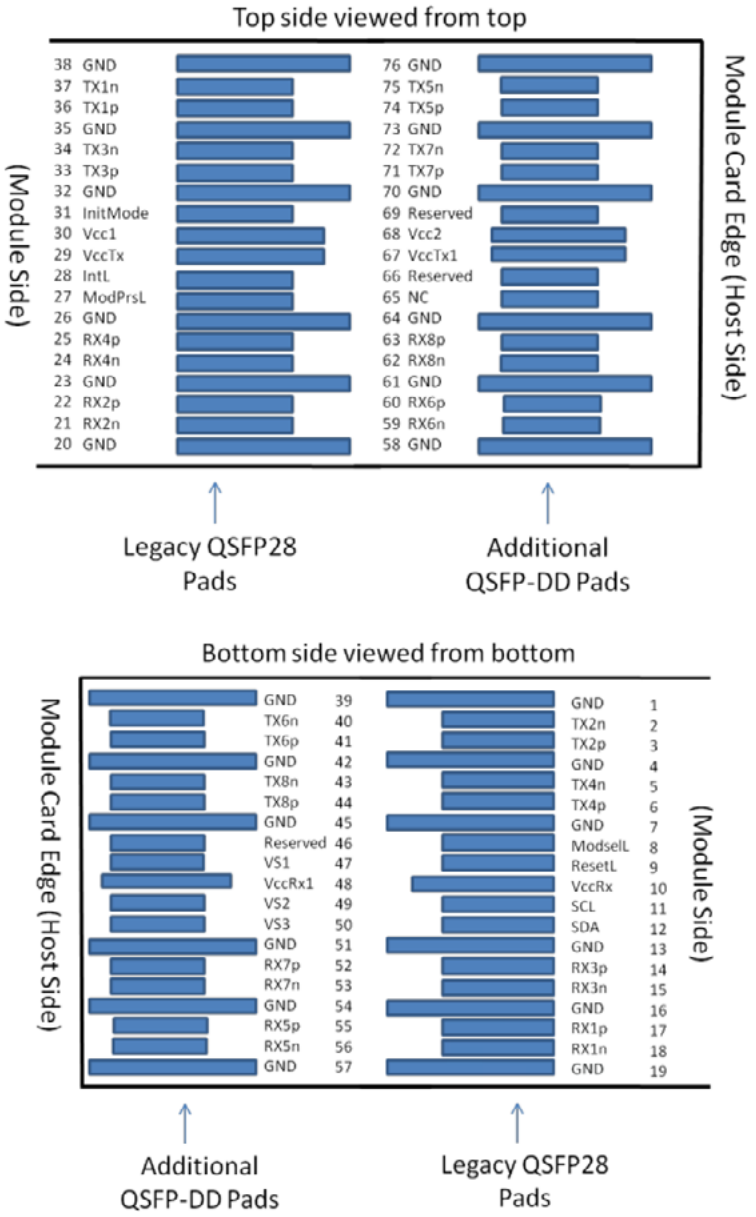
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
400G LR4 (10KM PRODUCT VARIANT)						
Average receive power, each lane		-9.1	-	5.6	dBm	
Receive power in OMA_{outer}, each lane		4.5	-	-	dBm	
Damage threshold, each lane		-	-	6.1	dBm	1
Receiver reflectance		-	-	-26	dB	
Unstressed receiver sensitivity (OMA_{outer}), each lane at pre-FEC BER of 2 x 10^{-4}	URS	max(-6.8, SECQ - 8.2),where 0.9 < SECQ < 3.9 dB (PRBS31Q)			dBM	2
Stressed receiver sensitivity (OMA_{outer}), each lane at pre-FEC BER of 2 x 10^{-4}	SRS	-	-	-4.3	dBM	
CONDITIONS OF STRESSED RECEIVER SENSITIVITY TEST						
Stressed eye closure for PAM4 (SECQ), each lane	SECQ	3.9			dB	3
OMA_{outer} of each aggressor lane		0.5			dBm	3

(1) The receiver is able to tolerate, without damage, continuous exposure to a signal having this average optical power level.
(2) Unstressed receiver sensitivity is informative and is defined via the equation given, for a test transmitter SECQ up to 3.4 dB.
(3) These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Electrical PIN Assignment

The optical transceiver pinout is compliant with the QSFP-DD MSA specifications. Figure below shows the module connector pad layout, and table below lists and describes all the electrical pins of the module.

ELECTRICAL CONNECTOR PAD LAYOUT



QSFP-DD MODULE ELECTRICAL CONNECTOR PIN DEFINITIONS

PAD	LOGIC	SYMBOL	DESCRIPTION	PLUG SEQUENCE	NOTES
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply, Receiver	2B	2
11	LVCMOS-I/O	SCL	2 Wire Serial Interface Clock	3B	
12	LVCMOS-I/O	SDA	2 Wire Serial Interface Data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	

QSFP-DD MODULE ELECTRICAL CONNECTOR PIN DEFINITIONS CONT.

PAD	LOGIC	SYMBOL	DESCRIPTION	PLUG SEQUENCE	NOTES
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL/ RxLOS	Interrupt	3B	
29		VccTx	+3.3V Power Supply Transmitter	2B	2
30		Vcc1	+3.3V Power Supply	2B	2
31	LVTTL-I	InitMode	Initialization Mode; in legacy QSFP applications, this pad is called LPMode	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	3
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	3
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	+3.3V Power Supply, Receiver	2A	2

QSFP-DD MODULE ELECTRICAL CONNECTOR PIN DEFINITIONS CONT.

PAD	LOGIC	SYMBOL	DESCRIPTION	PLUG SEQUENCE	NOTES
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	3
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	3
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	3
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	3
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	3
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	3
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	3
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	3
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	+3.3V Power Supply Transmitter	2A	2
68		Vcc2	+3.3V Power Supply	2A	2
69		Reserved	For future use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	3
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	3

QSFP-DD MODULE ELECTRICAL CONNECTOR PIN DEFINITIONS CONT.

PAD	LOGIC	SYMBOL	DESCRIPTION	PLUG SEQUENCE	NOTES
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	3
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	3
76		GND	Ground	1A	1

Note 1: QSFP-DD uses common ground (GND) for all signals and power supply. All are common within the module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Receiver Electrical Characteristics Table. VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

Note 3: All Vendor-Specific, Reserved, and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor-Specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

Power Supply

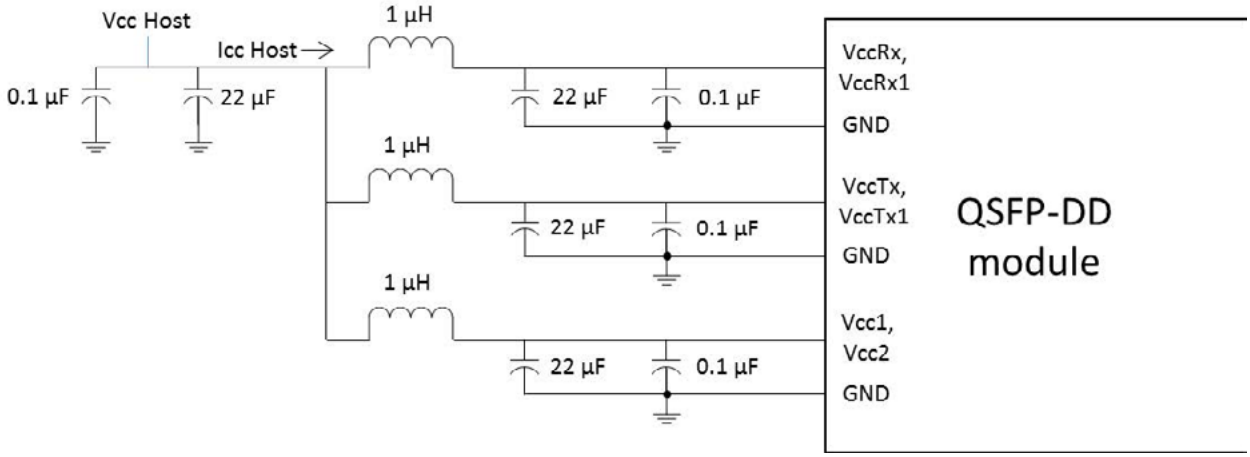
Here we describe the power supply filtering requirements and the power supply sequencing requirements.

POWER SUPPLY FILTERING

The power supply filtering requirements for the 400G FR4/LR4 QSFP-DD Optical Transceiver have been designed to be consistent with those required for QSFP-DD modules. A representative power supply filtering circuit is shown in the figure below: Recommended Power Supply Filtering Circuit.

One filtering circuit is recommended for each power supply rail.

RECOMMENDED POWER SUPPLY FILTERING CIRCUIT



POWER SUPPLY SPECIFICATIONS

Power supply specifications for the module are defined below. The module is compliant with QSFP-DD Power Class 5.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power supply voltages VccTx, VccTx1, VccRx, VccRx1, Vcc1, and Vcc2 (*)	VCC	3.135	3.3	3.465	V
Host RMS noise output 10 Hz – 10 MHz		-	-	25	mV
Module RMS noise output 10 Hz – 10 MHz		-	-	15	mV
Module power supply noise tolerance 10 Hz – 10 MHz (peak-to-peak)	$PSNR_{mod}$	-	-	66	mV
Module inrush – instantaneous peak duration	T_ip	-	-	50	µs
Module inrush – initialization time	T_init	-	-	500	ms

(*) Measured Including ripple, droop, and noise below 100 kHz

LOW POWER MODE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power consumption	P_lp	-	-	1.5	W
Instantaneous peak current at hot plug	Icc_ip_lp	-	-	600	mA
Sustained peak current at hot plug	Icc_sp_lp	-	-	495	mA
Steady state current	Icc_lp	-	-	478	mA

HIGH POWER MODE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power consumption	P_5	-	9	10	W
Instantaneous peak current at hot plug	Icc_ip_5	-	-	4000	mA
Sustained peak current at hot plug	Icc_sp_5	-	-	3300	mA
Steady state current	Icc_5	-	-	2727	mA

POWER SUPPLY SEQUENCING

No host power supply sequencing is required.

Control and Monitoring Interface

The optical transceiver supports a full QSFP-DD-compliant set of control, alarm, and monitoring features through a standard I^2C management interface, as well as low speed control pins which support additional module control and interrupt features.

LOW SPEED ELECTRICAL HARDWARE INTERFACE

In addition to the I^2C interface, the optical transceiver also supports low-speed control pins, which provide immediate easy access to key module functions and additional user interface signals to support the management interface.

ResetL

ResetL (LVTTL-I signal) is an input pin. The ResetL pin has a weak pull-up in the module to Vcc. A low level on the ResetL pin for longer than the minimum pulse length (t_reset_init > 2µs) initiates a complete module reset and returns all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the "Low" level signal on the ResetL pin is released.

ModPrsL

ModPrsL (LVTTL-O signal) is pulled up to Vcc on the host board and grounded in the module. The ModPrsL pin is asserted "Low" when the module is inserted and deasserted "High" when the module is physically absent from the host connector.

IntL

IntL (LVTTL-O signal) is an output signal. When IntL is asserted "Low," it indicates a possible module operational fault, LOS condition, or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface.

ModSelL

The ModSelL (LVTTL-I signal) is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. Otherwise, it does not. The ModSelL signal has a weak pull-up in the module connected to Vcc.

InitMode

InitMode (LVTTL-I signal) is an input signal. The InitMode signal allows the host to define whether the QSFP-DD module will initialize under host software control (InitMode asserted "High") or module hardware control (InitMode deasserted "Low"). Under host software control, the module shall remain in Low Power Mode until host software enables the transition to High Power Mode, as outlined in the Management Interface description below. Under hardware control, the module may immediately transition to High Power Mode after the management interface is initialized. The host shall not change the state of this signal while the module is present. In legacy QSFP applications, this signal is named LPMode. The InitMode signal has a weak pull-up in the module connected to Vcc.

SCL

The SCL pin (LVCMOS-I/O open-drain signal) is the 2-wire serial interface clock for the module. The SCL signal requires a pull-up resistor on the host board; ≤ 3 kΩ is recommended. Note that SCL and SDA timing specifications are defined in section defined in "Management Interface Timing."

SDA

The SDA pin (LVCMOS-I/O open-drain signal) is the 2-wire serial interface data for the module. The SDA signal requires a pull-up resistor on the host board; ≤ 3 kΩ is recommended. Note that SCL and SDA timing specifications are defined in section defined in "Management Interface Timing."

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
SCL and SDA	VOL	0	0.4	V	IOL_{max}=3 mA
	VOH	Vcc-0.5	Vcc+0.3		
	VIL	-0.3	Vcc*0.3		
	VIH	Vcc*0.7	Vcc+0.5		
Capacitance for SCL and SDA I/O signal	Ci	-	14	pF	
Total bus capacitive load for SCL and SDA	CB	-	100	pF	For 400 kHz clock frequency, max 3 kΩ pull up resistor
		-	200		For 400 kHz clock frequency, max 1.6 kΩ pull up resistor
InitMode, ResetL, and ModSelL	VIL	-0.3	0.8	V	
	VIH	2	Vcc+0.3		
	|Iin|	-	360	µA	OV < Vin < Vcc
IntL	VOL	0	0.4	V	IOL = 2 mA
	VOH	Vcc-0.5	Vcc+0.3		10kΩ pull up to Vcc
ModPrsL[1]	VOL	0	0.4	V	IOL = 2 mA

[1] ModPrsL can be implemented as a short-circuit to GND on the module

Management Interface

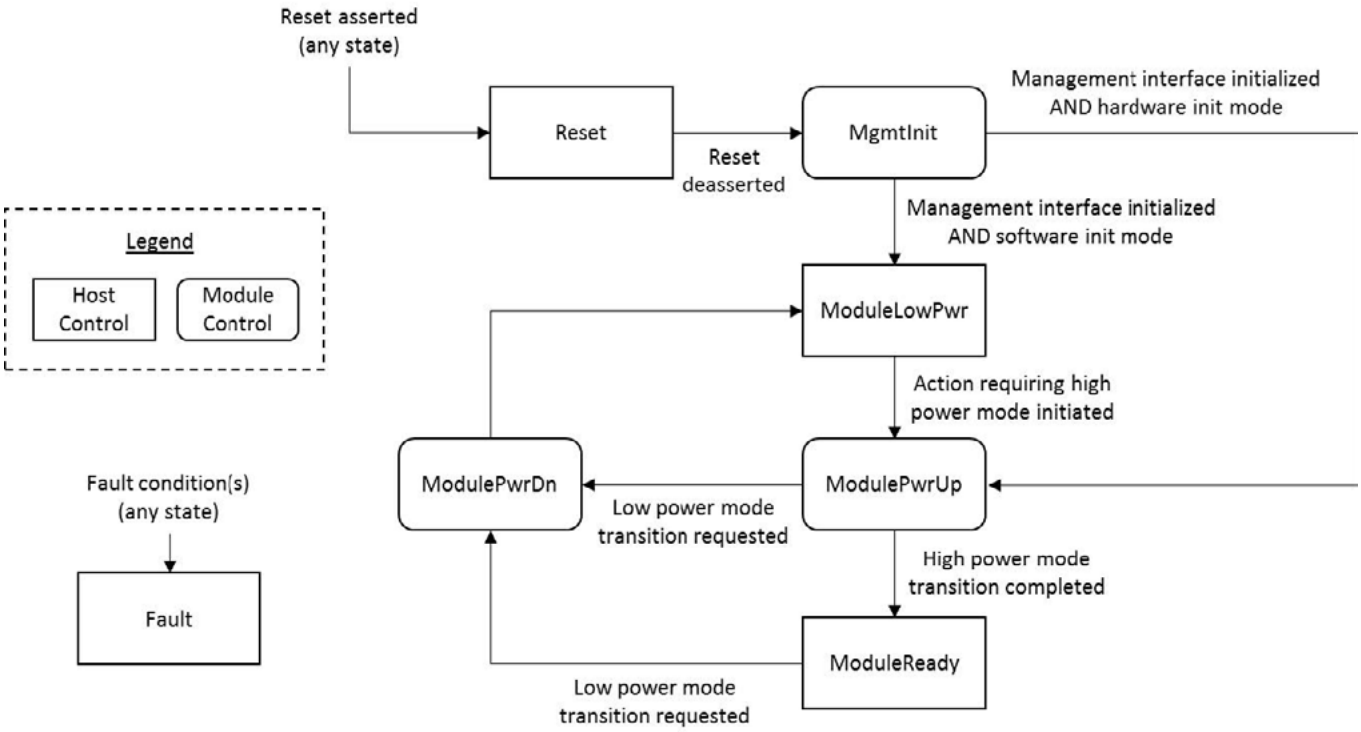
GENERAL FUNCTIONALITY

An I²C interface shall be used for management interface between the optical transceiver and the host system. The communication protocol shall follow the industry standard QSFP-DD management interface specification. Additional detail and clarified functionality is described in this sub-section.

MODULE STATE MACHINES

The module behavior during power-up, mode changes, and fault conditions complies with the Common Management Interface Specification (CMIS), as outlined in the state machine diagrams and descriptions below.

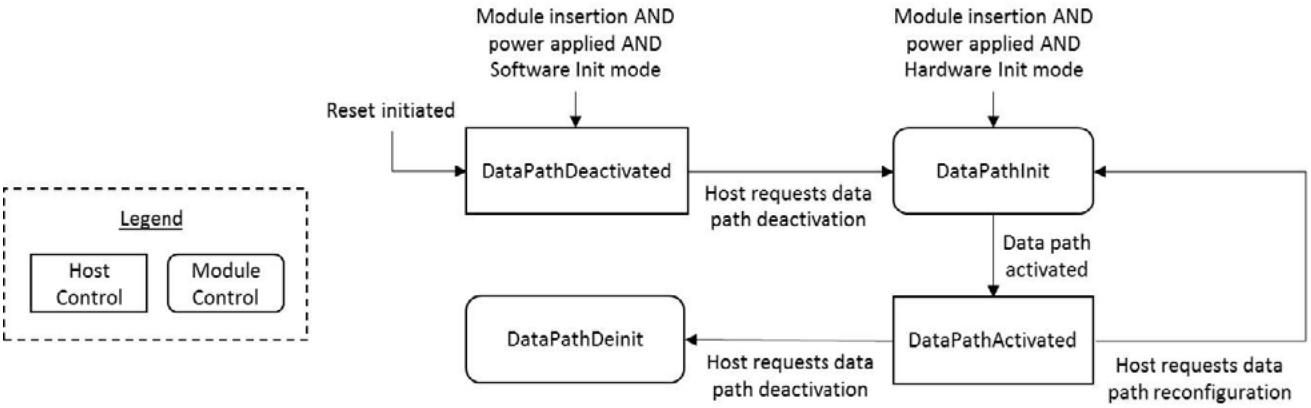
MODULE STATE MACHINE:



MODULE STATES BEHAVIOR

STATE	POWER MODE	EXIT CONDITION	INTERRUPT CLASS	DATA PATH STATE
Reset	Low power	Reset signal deasserted	Suppress all	DataPathDeactivated
MgmtInit	Low power	Module management interface ready AND interrupt signal asserted OR 2s timeout	Suppress all	DataPathDeactivated
ModuleLowPwr	Low power	Host requests an action that requires high power mode	All module flags permitted	DataPathDeactivated
ModulePwrUp	High power	Power up activities are complete	Suppress all	DataPathInit
ModuleReady	High power	Host requests module return to low power mode	All module flags permitted	Varies
ModulePwrDn	High power	Module has returned to low power mode	Suppress all	DataPathDeinit
Fault	Low power	Module reset or power down		DataPathDeactivated

MODULE DATA PATH STATE MACHINE



DATA PATH STATE BEHAVIORS

STATE	TX OUTPUT STATE	RX OUTPUT STATE	INTERRUPT CLASS	EXIT CONDITION
DataPathDeactivated	Quiescent	Quiescent	Suppress all data path flags	Host sets DataPathPwrUp bit(s)
DataPathInit	Quiescent	Quiescent	Suppress all	Module completes data path power up and initialization
DataPathActivated	See Byte 54h	Active	All data path flags permitted	1) Host clears DataPathPwrUp bit(s) AND module is active 2) Host requests data path reconfiguration
DataPathDeinit	Quiescent	Quiescent	Suppress all	Data path decommissioning complete

MANAGEMENT INTERFACE (I^2C) TIMING

Timing and other specs for the I^2C communication/management interface are given in the table below.

STATE	SYMBOL	MIN	MAX	MIN	MAX	UNIT	CONDITIONS
Clock Frequency	fSCL	0	400	0	1000	kHz	
Clock Pulse Width Low	tLOW	1.3	-	0.50	-	µs	
Clock Pulse Width High	tHIGH	0.6	-	0.26	-	µs	
Time bus free before new transmission can start	tBUF	20	-	1	-	µs	Between STOP and START and between ACK and Restart
START Hold Time	tHD.STA	0.6	-	0.26	-	µs	Delay required between SCL becoming low and SDA starting to go low in a START
START Setup Time	tSU.STA	0.6	-	0.26	-	µs	Delay required between SCL becoming low and SDA starting to go low in a START
Data In Hold Time	tHD.DAT	0	-	0	-	µs	
Data In Setup Time	tSU.DAT	0.1	-	0.1	-	µs	
Input Rise Time	tR		300		120	ns	From VIL to VIH
Input Fall Time	tF		300		120	ns	From VIH to VIL
STOP Setup Time	tSU.STO	0.6	-	0.26	-	µs	
STOP Hold Time	tHD.STO	0.6	-	0.26	-	µs	
Aborted sequence – bus release	Deselect_ Abort	2	-	2	-	ms	Delay from a host deasserting ModSelL (at any point in a bus sequence) to the module releasing SCL and SDA
ModSelL Setup Time	tSU.ModSelL	2	-	2	-	ms	Setup time on the select lines before the start of a host initiated serial bus sequence
ModSelL Hold Time	tHD.ModSelL	2	-	2	-	ms	Delay from completion of a serial bus sequence to changes of module select status
Serial Interface Clock Holdoff “Clock Stretching”	T_clock_hold	-	500	-	500	µs	Maximum time the module may hold the SCL line low before continuing with a read or write operation
Complete Single or Sequential Write	tWR	-	40	-	40	ms	Complete (up to) 4 byte write
Endurance (Write Cycles)		50k	-	50k	-	cycles	Module case temperature = 70C

SOFT CONTROL, ALARM, AND STATUS TIMING

Timing specifications for control inputs and alarm/warning and status indicators follow QSFP-DD MSA Hardware specification rev 5.0.

FAULT BEHAVIOR

The Tx Fault indicator of the module will trigger (Tx Fault bit set to 1) when any of the Tx High or Low Output Power alarms, Tx Loss of Lock alarm, or the Tx Bias Current High or Low alarms are triggered. Any of the contributing alarm conditions may be masked per the mask control registers provided in the corresponding module EEPROM/memory registers.
The Rx LOS indicator of the module will assert when the Rx Low Power alarm asserts, and it will deassert when the Rx Low Power alarm deasserts. For Rx Low Power alarm threshold values, see the corresponding module memory map registers.

MECHANICAL SPECIFICATIONS

The module is compliant with QSFP-DD mechanical specifications for a Type 2 QSFP-DD module. The module electrical connector is compliant with QSFP-DD specifications. The module optical connector is a standard LC connector.

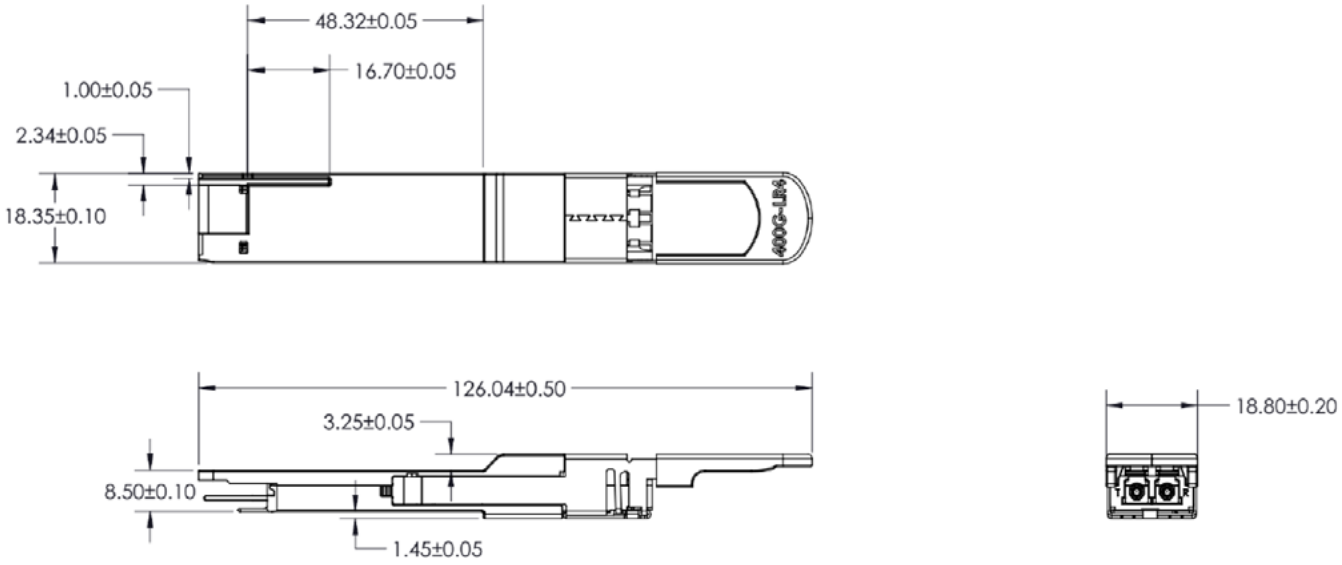
MONITOR ACCURACY

The module analog monitors have accuracy as defined below.

MONITOR	ACCURACY
RX input power monitor	+/- 3 dB
TX output power monitor	+/- 3 dB
TX bias current monitor	+/- 10%
Case temperature monitor	+/- 3C
Supply voltage monitor	+/- 10%

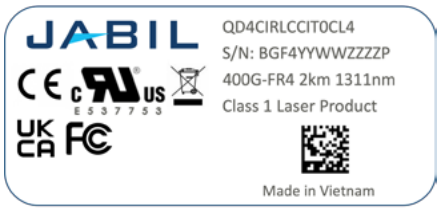
REGISTER MAPPING

The module complies with the QSFP-DD memory map specification (under development by the MSA group).



Label Specification

The following printed label is attached to the product (note that the certification labels will be added/removed according to requests and certification process results):



Regulatory and Compliance

EMC — Immunity	• EN 55024 (EU) • IEC EN 61000-4-3 (International)	• EMC Directive 89/336/EEC • IEC /CISPR/24
EMC — Emission	• CISPR 22, class B (Comité International Spécial des Perturbations Radioélectriques--CISPR; Special international committee on radio interference. International). • AS/NZS CISPR22 (Australia/New Zealand)	• VCCI-03 (Japan) • FCC 47 CFR Part 15, class B (US) • ICES-003, Issue 4 (Canada) • EN 55022 (EU) • EMC Directive 2004/108/EEC (EU)
ESD Threshold	• Per MIL-STD 883C Method 3015.4 or ANSI/ESDA/JEDEC JS-001-2012 (component level). • IEC EN 61000-4-2; +/- 8kV contact, +/- 15kV air.	
Product Safety	• UL Recognized Component: UL 60950-1 (2nd Ed.) Information Technology Equipment; CAN/CSA-C22.2 No. 60950-1 (2007) Information Technology Equipment; UL94-V0 flammability. • CB Certificate: IEC 60950-1 (2005 +A1:2009) Information Technology Equipment.	
Fire Safety	• PCB material must be fully compliant to UL796; Temperature class B (IEC 60085); flammability class V-0- UL94). • Cables and connectors must have a flammability ratings of V0- UL94; Service temp.≥90 C. • Label materials must have a flammability ratings of V0- UL94; Service temp.≥90 C. • Optical fibers must have a flammability ratings of V0- UL94; Service temp.≥85 C.	

Optical Safety	• FDA/CDRH certified with accession number, Class 1 laser product:
	  • U.S. 21 CFR 1040;
	  • UL mark
	• UL Certificate:
	  • IEC 60825-1:2014;
	  • EN 60825-1:2014 + A11:2021
		• Complies with 21 CFR 1040.10 and 1040.11 except for conformance with IEC 60825-1 Ed. 3., as described in Laser Notice No. 56, dated May 8, 2019.
		• Caution – Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

RoHS	• 2002/95/EC and the revised and recast Directive 2011/65/EC (RoHS) Restriction on Hazardous Substances. • 2006/1907/EC (REACH) Registration, Evaluation, Authorization of Chemicals.	• JIG 101-A, JIG 101-B Joint Industry Guide Japanese Material Composition Declaration. • CAITEC SJ/T 11363-2006 Requirements for Concentration Limits for Certain Hazardous Substances in Electronic Information Products (China RoHS) • Complies with RoHS II Directive 2011/65/EU.

For additional information, visit jabil.com

Ordering Information

JABIL PART NUMBER		PACKAGE	RATE	REACH	OTHER INFO
QD4CIRLCCxx0CL4	400 Gb/s FR4 QSFP-DD Optical Transceiver with LC connector, 2km Reach	QSFP-DD	425G	2 km	C-Temp
QD4CLRLCCxx0CL4	400 Gb/s LR4 QSFP-DD Optical Transceiver with LC connector, 10km Reach	QSFP-DD	425G	10 km	C-Temp

Document Version

VERSION	DATE	NOTES
1.0	11/21/2023	Initial specification version
1.1	02/29/2024	Added LR4 specification
1.2	07/08/2024	Updated Regulatory and Compliance

Manufacturer's Address

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