100G QSFP28 DR1 Optical Transceiver

Jabil 100 Gb/s DR1 QSFP28 Optical Transceiver is a small form-factor, high speed, and low-power consumption product targeted for use in optical interconnects for data communications applications. The high-bandwidth QSFP28 module supports 500 m links over single-mode fiber via LC connector.

FEATURES

- Compliant to 100G DR1 optical interface specification per 100G Lambda MSA and IEEE 802.3, with reach up to 500 m
- Compact QSFP28 form factor for high faceplate density in networking equipment
- Compatibility with SMF connectors and cable infrastructures
- Application supports operation with Forward Error Correction (FEC)
- CAUI-4 compliant electric interface per IEEE 802.3
- Power dissipation < 3.5W
- Operating temperature range: 0° to 70°C
- Full module diagnostics and control through I2C, compliant with SFF-8636
- Single 3.3V power supply
- RoHS-6 compliance

APPLICATIONS

- 100GbE connectivity for large-scale cloud and enterprise data centers
- Ethernet switch, router, and client-side telecom interfaces

STANDARDS

- QSFP28 MSA
- IEEE 802.3bm

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Storage Temperature	Ts	-40	+85	ºC
Case Operating Temperature	Tc	-5	75	ºC
Relative Humidity (*)	RH	5	85	%
DC Supply Voltage	V_{CC}	-	3.6	V
ESD (HBM)	V_{ESD}	-1k	1k	V
Differential Input Voltage	$V_{in\text{-}pp}$	-	1600	mVpp
Receiver Input Optical Power	P_{IN} (max)	-	+3.5	dBm

(*) not condensing

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Operating Case Temperature	TCASE	0	30	70	°C
DC Supply Voltage	V_{CC}	3.14	3.3	3.47	V
Power Supply Noise Tolerance (*)		-	-	66	mVpp
Bit Rate	BR	-	25.8	-	Gbps

(*) At input to recommended power supply filter

LOW-SPEED ELECTRICAL SPECIFICATIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power consumption	Pcon	-	-	3.5	W
Control input high	Vih	+2.8	-	+3.3	V
Control input low	Vil	-0.3	-	+0.8	V
Control output high	Voh	+2.8	-	+3.3	V
Control output low	Vol	0.0	-	+0.4	V
Control output current (*)		-	-	30	mA
LOS output current		-	-	30	mA
SDA, SCL min sink current (**)		-	-	3	mA

(*) IntL
(**) Requires a host board pull-up to Vcc of 5kΩ or less.

Optical Transmitter

The 100G DR1 optical transceiver electric interface is based on IEEE 802.3 CAUI-4 host to module retimed interface. Optical transmitter/receiver specifications are compliant with 100G DR specification.

TRANSMITTER ELECTRICAL INPUT CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data rate		-	25.8	-	Gbps	
DC common mode voltage	V_{in_CM}	-400	-	2850	mV	
Differential termination mismatch		-	-	10	%	
Tx differential Input swing	Vin_pp	300	-	900	mV	
Single-ended voltage tolerance	Vin_se	-0.4	-	3.3	V	
Tx input channel loss	CL	-	-	10	dB	Chip-to-chip @ 12.9 GHz
Electrical interface BER		-	-	1e-15		With stressed input signal per IEEE802.3bm Annex 83E.3.4.2
Differential input return loss		Minimum per IEEE802.3bm Annex 83E.				
Different to common mode input return loss		Minimum per IEEE802.3bm Annex 83E.	-			

TRANSMITTER OPTICAL OUTPUT CHARACTERISTICS (WITH FEC)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data rate		106.24	106.25	106.26	Gbps	
Baud/symbol rate	BR	53.12	53.125	53.13	GBd	
Lane wavelength range		1304.5 to 1317.5 1311 center wavelength			nm	
Side mode suppression ratio	SMSR	30	-	-	dB	
Average optical output power	P_{ave}	-2.9	-	4	dBm	
Extinction ratio	ER	3.5	-	-	dB	
Optical modulation amplitude	OMA_{outer}	-0.8	-	4.2	dBm	
Transmitter dispersion and eye closure penalty	TDECQ	-	-	3.4	dB	
OMA minus TDECQ		-2.2	-	-	dBm	
Transmitter transition time	Tr, Tf			17	ps	
Average optical output power of OFF transmitter		-	-	-30	dBm	
Transmitter reflectance		-	-	-26	dB	
$RIN_{17.1}OMA$	RIN	-	-	-136	dB/Hz	
Optical return loss tolerance	ORLT	-	-	17.1	dB	
Operating link reach		2	-	500	m	

Optical Receiver

RECEIVER ELECTRICAL OUTPUT CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data rate			25.8		Gbps	
DC common mode voltage	$V_{out\_DC\text{-}CM}$	-400	-	2850	mV	
AC common mode voltage (rms)	$V_{out\_AC\text{-}CM}$	-	-	17.5	mVrms	
Rx output data total jitter	TJ_{Rxout}	-	-	0.63	UI	
SDD22, SDC22, SCD22 and SCC22	As per CEI-28G-VSR at TP4					
Rx output data raise time (20-80%)		9.5	-	-	ps	
Rx output data fall time (20-80%)		9.5	-	-	ps	
Eye width at 10^{-15}	EW15	0.57	-	-	UI	
Eye height at 10^{-15}	EH15	228	-	-	mV	
Differential output return loss	SDD22	Per IEEE802.3bm Annex 83E				
Common to differential mode conversion return loss	SCD22	Per IEEE802.3bm Annex 83E				

RECEIVER OPTICAL INPUT CHARACTERISTICS

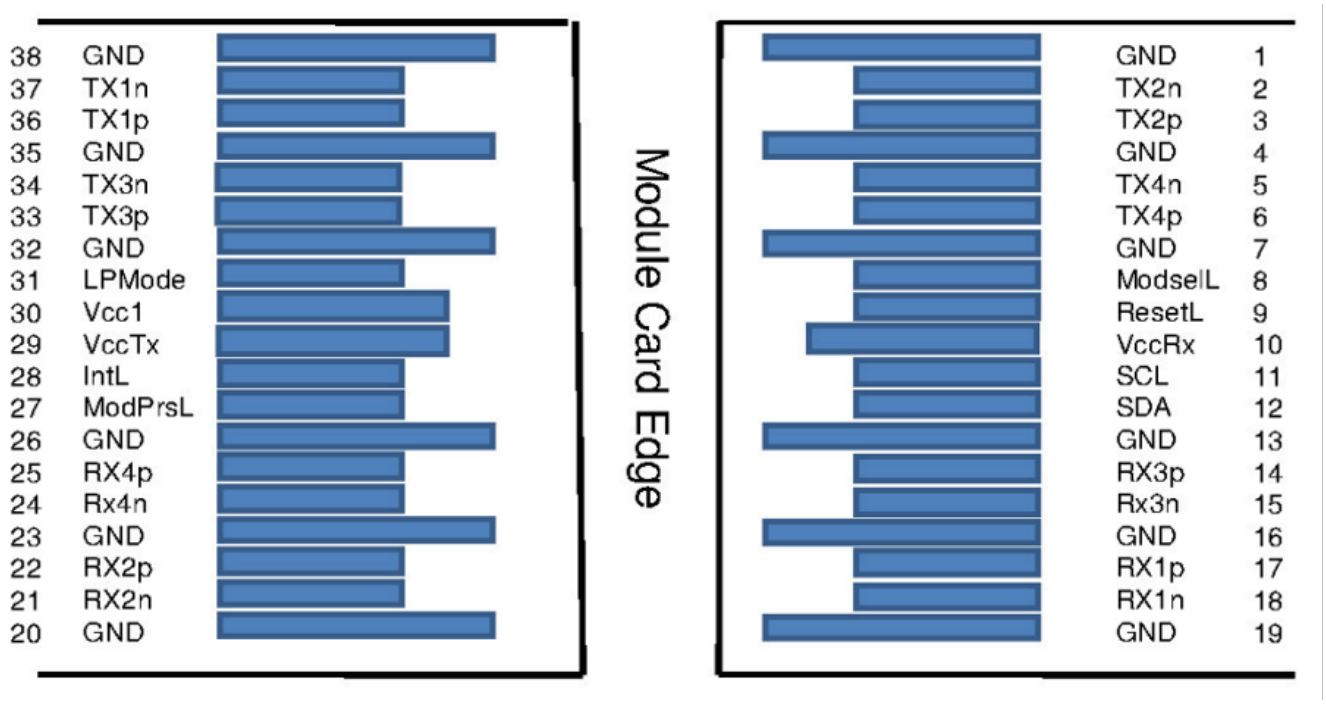
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data modulation type			PAM4			
Data rate	BR	106.24	106.25	106.26	Gbps	
Baud/symbol rate, each lane	BR	53.12	53.125	53.13	Gbd	
Lane wavelengths		1304.5 to 1317.5 1311 center wavelength			nm	
Bit error rate, uncorrected	BER_{pre}			2×10^{-4}		
Bit error rate, corrected	BER_{post}			1×10^{-15}		
Average receive power		-5.9	-	4	dBm	
Receive power	OMA_{outer}	-	-	4.2	dBm	
Damage threshold		-	-	5	dBm	
Receiver reflectance		-	-	-26	dB	
Unstressed receiver sensitivity (OMAouter), each lane at pre-FEC BER of 2×10^{-4}	URS	max(-3.9, SECQ - 5.3)			dBm	1
Stressed receiver sensitivity (OMAouter), each lane at pre-FEC BER of 2×10^{-4}	SRS	-	-	-1.9	dBm	1
CONDITIONS OF STRESSED RECEIVER SENSITIVITY TEST						
Stressed eye closure for PAM4 (SECQ)	SECQ	3.4			dB	2

(1) URS is informational.
(2) These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Electrical PIN Assignment

The 100 Gbps DR1 QSFP28 optical transceiver pinout is compliant with the QSFP specifications in SFF-8436. The table below lists and describes all of the electrical pins of the module.

ELECTRICAL CONNECTOR PAD LAYOUT



TOP SIDE
VIEWED FROM TOP

BOTTOM SIDE
VIEWED FROM BOTTOM

QSFP28 MODULE ELECTRICAL CONNECTOR PIN DEFINITIONS

PAD	LOGIC	SYMBOL	DESCRIPTION	PLUG SEQUENCE	NOTES
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		VccRx	+3.3V Power Supply, Receiver	2	2
11	LVCMOS-I/O	SCL	2 Wire Serial Interface Clock	3	
12	LVCMOS-I/O	SDA	2 Wire Serial Interface Data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	

QSFP28 MODULE ELECTRICAL CONNECTOR PIN DEFINITIONS CONT.

PAD	LOGIC	SYMBOL	DESCRIPTION	PLUG SEQUENCE	NOTES
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL/ RxLOS	Interrupt	3	
29		VccTx	+3.3V Power Supply Transmitter	2	2
30		Vcc1	+3.3V Power Supply	2	2
31	LVTTL-I	InitMode	Initialization Mode; in legacy QSFP applications, this pad is called LPMode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Note 1: GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the host edge card connector are listed in Table 6. Recommended host board power supply filtering is shown in Figures 3 and 4. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP+ module in any combination. The connector pins are each rated for a maximum current of 500 mA.

Power Supply

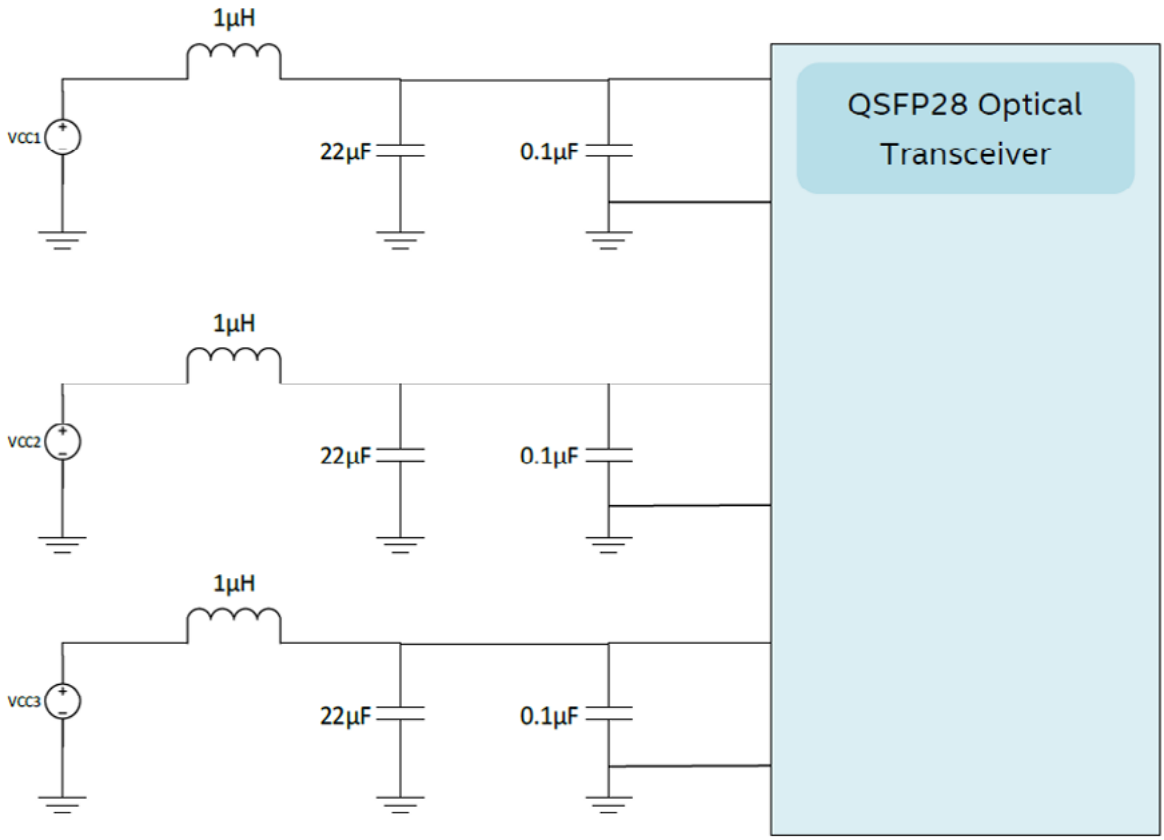
Here we describe the power supply filtering requirements and the power supply sequencing requirements.

POWER SUPPLY FILTERING

The power supply filtering requirements for the 100 Gbps DR1 QSFP28 optical transceiver have been designed to be consistent with those required for QSFP modules. A representative power supply filtering circuit is shown in figure below.

One filtering circuit is recommended for each power supply rail.

RECOMMENDED POWER SUPPLY FILTERING CIRCUIT



POWER SUPPLY SEQUENCING

No host power supply sequencing is required.

Control and Monitoring Interface

The 100 Gbps DR1 QSFP28 Optical Transceiver hardware pins support a full SFF-8436 and SFF-8636–compliant set of control, alarm, and monitoring features through a standard I2C management interface, as well as low speed control pins, which support additional module control and interrupt features.

LOW-SPEED ELECTRICAL HARDWARE INTERFACE

In addition to the I^2C interface, the optical transceiver also supports low-speed control pins, which provide immediate easy access to key module functions and provide additional user interface signals to support the management interface.

ResetL

ResetL (LVTTL-I signal) is an input pin. The ResetL pin has a weak pull-up in the module to Vcc. A low level on the ResetL pin for longer than the minimum pulse length (t_reset_init > 2µs) initiates a complete module reset and returns all user module settings to their default state. Module reset assert time (t_init) starts on the rising edge after the "low" level signal on the ResetL pin is released.

ModPrsL

ModPrsL (LVTTL-O signal) is pulled up to Vcc on the host board and grounded in the module. The ModPrsL pin is asserted "low" when the module is inserted and deasserted "high" when the module is physically absent from the host connector.

IntL

IntL (LVTTL-O signal) is an output signal. When IntL is asserted "low," it indicates a possible module operational fault, LOS condition, or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface.

ModSelL

The ModSelL (LVTTL-I signal) is an input pin. When held low by the host, the module responds to 2-wire serial communication commands, otherwise it does not. The ModSelL signal has a weak pull-up in the module connected to Vcc.

LPMode

LPMode (LVTTL-I signal) is an input signal. When LPMode is set "low," the module will boot into its standard default state. When LPMode is set "high," the module will boot into "low power mode" and only the management interface is active (high-speed TX and RX are shut down). The LPMode signal has a weak pull-up on the module connected to Vcc.

SCL

The SCL pin (LVCMOS-I/O open-drain signal) is the 2-wire serial interface clock for the module. The SCL signal requires a pull-up resistor on the host board, ≤ 5 kΩ is recommended.

SDA

The SDA pin (LVCMOS-I/O open-drain signal) is the 2-wire serial interface data for the module. The SDA signal requires a pull-up resistor on the host board, ≤ 5 kΩ is recommended.

Management Interface

GENERAL FUNCTIONALITY

An I^2C interface shall be used for management interface between the optical transceiver and the host system. The communication protocol shall follow the industry standard SFF-8636 specification for common management interface. Additional detail and clarified functionality are described in this sub-section.

MONITOR ACCURACY

The 100G DR1 module analog monitors have accuracy as defined below.

MONITOR	ACCURACY
RX input power	+/- 3 dB
TX output power	+/- 3 dB
TX bias current	+/- 10%
Module temperature	+/- 3C
Module supply voltages	+/- 3%

REGISTER MAPPING

The module complies with the SFF-8636 memory map specification for a QSFP28 module.

FROM	TO	CONTENT	NO. OF BYTES	TYPE
		Lower Page 00h		
0	2	ID and Status	3	Read-Only
3	21	Interrupt Flags (Clear on read)	19	Read-Only
22	33	Free Side Device Monitors	12	Read-Only
34	81	Channel Monitors	48	Read-Only
82	85	Reserved	4	Read-Only
86	99	Control	14	Read/Write
100	106	Free Side Interrupt Masks	7	Read/Write
107	110	Free Side Device Properties	4	Read-Only
111	112	Assigned to PCI Express	2	Read/Write

REGISTER MAPPING CONT.

FROM	TO	CONTENT	NO. OF BYTES	TYPE
113	116	Free Side Device Properties	4	Read-Only
117	118	Reserved	2	Read/Write
119	122	Optional Password Change	4	Write-Only
123	126	Optional Password Entry	4	Write-Only
127	127	Page Select Byte	1	Read/Write
		Upper Page 00h		
128	128	Identifier	1	Read-Only
129	191	Base ID Fields	63	Read-Only
192	223	Extended ID	32	Read-Only
224	255	Vendor Specific ID	32	Read-Only
		Page 02h (user EEPROM)		
128	255	User EEPROM Data	128	Read/Write
		Page 03h (Module and lane thresholds, masks, controls)		
128	175	Free Side Device Thresholds	48	Read-Only
176	223	Channel Thresholds	48	Read-Only
224	229	Tx EQ, Rx Output and TC Support	6	Read-Only
230	241	Channel Controls	12	Read/Write
242	251	Channel Monitor Masks	10	Read/Write
252	255	Reserved	4	Read/Write
		Page 13h		
128	255	Diagnostic Status and Counters	128	Read/Write
		Page 14h		
128	255	Diagnostic Advertising and Control	128	Read/Write
		Pages 20h-21h		
128	255	PAM-4 and WDM Features	128	Read/Write
		Pages 9Fh		
128	255	Command and Local Payload for CDB	128	Read/Write

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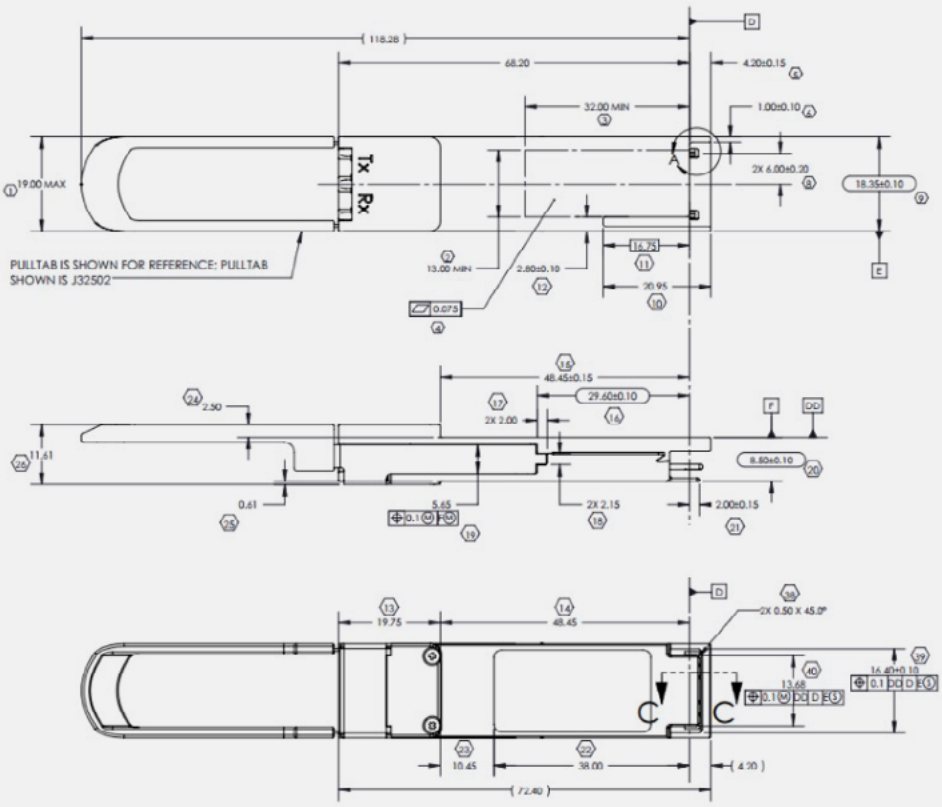
Mechanical Specifications

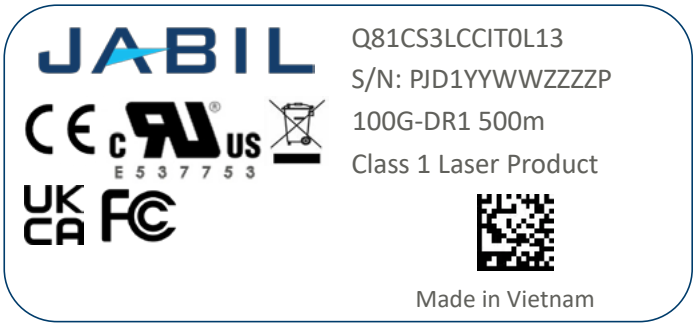
QSFP28 DIMENSIONS



Label Specification

The following printed label is attached to the product (note that the certification labels will be added/removed according to requests and certification process results):

:



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Regulatory and Compliance

EMC — Immunity	• EN 55024 (EU) • IEC EN 61000-4-3 (International)	• EMC Directive 89/336/EEC • IEC /CISPR/24
EMC — Emission	• CISPR 22, class B (Comité International Spécial des Perturbations Radioélectriques — CISPR; Special international committee on radio interference. International). • AS/NZS CISPR22 (Australia/New Zealand)	• VCCI-03 (Japan) • FCC 47 CFR Part 15, class B (US) • ICES-003, Issue 4 (Canada) • EN 55022 (EU) • EMC Directive 2004/108/EEC (EU)
ESD Threshold	• Per MIL-STD 883C Method 3015.4 or ANSI/ESDA/JEDEC JS-001-2012 (component level). • IEC EN 61000-4-2; +/- 8kV contact, +/- 15kV air.	
Product Safety	• UL Recognized Component: UL 60950-1 (2nd Ed.) Information Technology Equipment; CAN/CSA-C22.2 No. 60950-1 (2007) Information Technology Equipment; UL94-V0 flammability. • TUV Bauart Certificate: EN 60950-1 (2006+ A12:2012) Information Technology Equipment. • CB Certificate: IEC 60950-1 (2005 +A1:2009) Information Technology Equipment.	
Fire Safety	• PCB material must be fully compliant to UL796; Temperature class B (IEC 60085); flammability class V-0- UL94). • Cables and connectors must have a flammability ratings of V0- UL94; Service temp.≥ 90 C. • Label materials must have a flammability ratings of V0- UL94; Service temp.≥ 90 C. • Optical fibers must have a flammability ratings of V0- UL94; Service temp.≥ 85 C.	

Optical Safety	• FDA/CDRH certified with accession number, Class 1 laser product:
	  • U.S. 21 CFR 1040;
	  • UL mark
	• UL Certificate:
	  • IEC 60825-1:2014;
	  • EN 60825-1:2014 + A11:2021
		• Complies with 21 CFR 1040.10 and 1040.11 except for conformance with IEC 60825-1 Ed. 3., as described in Laser Notice No. 56, dated May 8, 2019.
		• Caution – Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

RoHS	• 2002/95/EC and the revised and recast Directive 2011/65/EC (RoHS) Restriction on Hazardous Substances. • 2006/1907/EC (REACH) Registration, Evaluation, Authorization of Chemicals.	• JIG 101-A, JIG 101-B Joint Industry Guide Japanese Material Composition Declaration. • CAITEC SJ/T 11363-2006 Requirements for Concentration Limits for Certain Hazardous Substances in Electronic Information Products (China RoHS) • Complies with RoHS II Directive 2011/65/EU.

For additional information, visit jabil.com

Ordering Information

JABIL PART NUMBER		PACKAGE	RATE	REACH	OTHER INFO
Q81CS3LCCxx0L13	100 Gb/s DR1 QSFP28 Optical Transceiver with LC connector, 500m Reach	QSFP28	106.25G	500m	C-Temp

Document Version

VERSION	DATE	NOTES
1.0	11/24/2023	Initial specification version
1.1	7/8/2024	Updated Regulatory and Compliance

Manufacturer's Address

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