JABIL

200G QSFP56 FR4 PAM4 Optical Transceiver

Jabil 200 Gb/s QSFP56 FR4 PAM4 Optical Transceiver is a small form-factor, high speed, and low power consumption product targeted for use in optical interconnects for data communications applications. The high bandwidth QSFP56 module supports 2 km links over single-mode fiber via LC connector.

FEATURES

- Compliant to FR4 MSA and IEEE 802.3bs 200GAUI-4 (CAUI-4) optical and electrical interface specifications, with reach up to 2 km
- Compact QSFP56 form factor for high faceplate density in networking equipment
- Compatibility with single-mode optical connectors and cable infrastructures
- Operating temperature range: 0 to 70°C
- CMIS-compliant management interface with full module diagnostics and control through I2C
- Single 3.3V Power supply
- Power consumption < 6.5W
- RoHS-6 Compliance

APPLICATIONS

- 200GbE connectivity for large-scale cloud and enterprise data centers
- Ethernet switch, router, and client-side telecom interfaces

STANDARDS

- · QSFP56 MSA
- IEEE 802.3bs

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Storage Temperature	Tstg	-40	+85	^o C
Case Operating Temperature	TOP	-5	70	^o C
Relative Humidity	RH	5	85	%
DC Supply Voltage	VCC	-	3.6	V
ESD (HBM)	VESD	-1k	1k	V
Receiver Damage Threshold	P_rx (max)	-	5.7	dBm

^(*) not condensing

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Case Operating Temperature	TCASE	0		70	°C
DC Supply Voltage	t	3.135	3.3	3.465	V
Power Supply consumption (200G Mode)				6.5	W
Power Supply Noise Tolerance (*)		-	-	66	mVpp
Bit Rate	BR	53.12	53.125	53.13	Gbps

^(*) At input to recommended power supply filter

Optical Transmitter

The 200G FR4 optical transceiver electrical interface is compliant to the IEEE 802.3bs 200GAUI-4 (CDAUI-4) host to module retimed interface. Optical transmitter/receiver specifications are compliant with IEEE 802.3bs 200GBASE-FR4 specification based on duplex SMF with optical ach of 2km.

TRANSMITTER ELECTRICAL INPUT CHARACTERISTICS (TP1)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data modulation type			PAM4			
Data rate, each lane	BR	53.119	53.125	53.13	Gbps	
Baud/symbol rate, each lane	BR	26.559	26.5625	26.565	Gbd	
DC common mode voltage	Vin_CM	-350	-	2850	mV	
Differential input return loss	SDD11	Per IEEE802.3bm Annex 83E, Equation 83E-5				
Differential to common mode input return loss	SDC11	Per IEEE802.3bm Annex 83E, Equation 83E-6				
Differential termination mismatch		-	-	10	%	

TRANSMITTER OPTICAL OUTPUT CHARACTERISTICS (TP2)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data modulation type			PAM4			
Data rate, each lane	BR	53.12	53.125	53.13	Gbps	
Baud/symbol rate, each lane	BR	26.56	26.5625	26.565	Gbd	
		1265.25	1271	1276.75		
Languagalanatha	\\\\	1285.25	1291	1296.75		
Lane wavelengths	WL	1305.25	1311	1316.75	nm	
		1325.25	1331	1336.75		
Side mode suppression ratio	SMSR	30	-	-	dB	
Average optical output power, each lane	Pave	-4.2	-	4.7	dBm	1
Total Ave Launch Power	AOPtot			10.7	dBm	
Optical modulation amplitude, each lane	OMA _{outer}	-1.2	-	4.5	dBm	
Transmitter dispersion and eye closure penalty, each lane	TDECQ	-	-	4	dB	
OMA minus TDECQ, each lane		-2.5	-	-	dBm	2
Extinction Ratio	ER	3.5	-	-	dB	
Average optical output power of OFF transmitter, each lane		-	-	-30	dBm	
Transmitter reflectance		-	-	-26	dB	3
RIN20 OMA	RIN	-	-	-132	dB/Hz	4
Optical Return Loss Tolerance	ORLT	-	-	16.5	dB	
Operating link reach		2	-	2000	m	

⁽¹⁾ Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance

⁽²⁾ Even if the TDECQ < 1.4 dB for an extinction ratio of \geq 4.5 dB or TDECQ < 1.3 dB for an extinction ratio of < 4.5 dB, the OMAouter must exceed this value

⁽³⁾ Transmitter reflectance is defined looking into the transmitter

⁽⁴⁾ RIN on OMA measured with 17.1dB return loss

Optical Receiver

RECEIVER ELECTRICAL OUTPUT CHARACTERISTICS (TP4)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Data modulation type			PA	M4	
Data rate, each lane	BR	53.119	53.125	53.13	Gbps
Baud/symbol rate, each lane	BR	26.559	26.5625	26.565	Gbd
DC common mode voltage	Vout_AC-CM	-350	-	2850	mV
AC common mode voltage (rms)	Vout_DC-CM	-	-	17.5	mVrms
Differential peak-to-peak output voltage	Vout_pp	-	-	900	mVpp
Near-end ESMW (eye symmetry mask width)	ESMWnear		0.265		UI
Near-end eye height, differential	EH _{near}	70	-	-	mV
Far-end ESMW (eye symmetry mask width)	ESMW _{far}		0.2		UI
Far-end eye height, differential	EHfar	30	-	-	mV
Far-end pre-cursor ISI ratio		-4.5	-	2.5	%
Differential output return loss	SDD22	Per IEEE802.3bm Annex 83E			
Common to differential mode conversion return loss	SCD22	Per IEEE802.3bm Annex 83E			
Differential termination mismatch		-	-	10	%

RECEIVER OPTICAL INPUT CHARACTERISTICS (TP3)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data modulation type			PAM4			
Data rate, each lane	BR	53.12	53.125	53.13	Gbps	
Baud/symbol rate, each lane	BR	26.56	26.5625	26.565	Gbd	
		1265.25	1271	1276.75	nm	
Lana wayalanatha	\\/\/	1285.25	1291	1296.75		
Lane wavelengths	WL	1305.25	1311	1316.75		
		1325.25	1331	1336.75		
Bit Error Rate, uncorrected/pre-FEC	BERpre	-	-	2.4 x 10 ⁻⁴		1
Average receive power, each lane		-8.2	-	4.7	dBm	2
Receive power in OMAouter, each lane		-	-	4.5	dBm	
Stressed Receiver Sensitivity (OMAouter), each lane at pre-FEC BER of 2 x 10-4	SRS	-	-	-3.6	dBm	3,4
Stressed eye closure for PAM4 (SECQ), each lane	SECQ	3.3			dB	
OMAouter of each aggressor lane			0.5		dBm	

⁽¹⁾ Measured with a reference transmitter to produce SECQ greater than or equal to 2dB. The BER at receiver must stay within the specified limit over an OMA range of -5.9dBm to 4.5dBm

⁽²⁾ Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

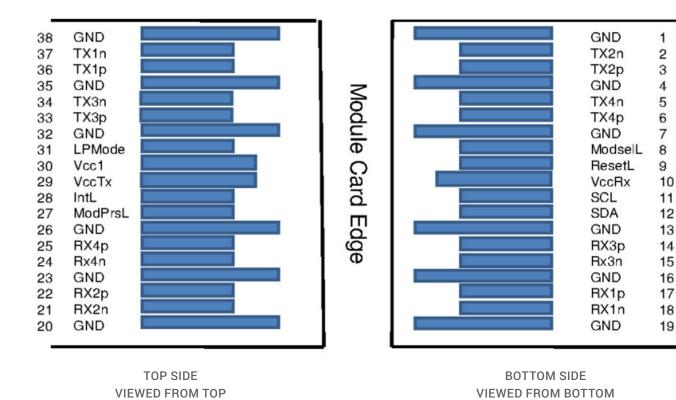
⁽³⁾ Receiver sensitivity (OMAouter), each lane is informative and is defined for a transmitter with SECQ of 0.9 dB.

⁽⁴⁾ Measured with conformance test signal at TP3 for the BER = 2.4E-4. The stressed conditions are: a). Stressed eye closure for PAM4 (SECQ), lane under test = 3.3 and b). OMAouter of each aggressor lane = 0.5

Electrical PIN Assignment

The optical transceiver pinout for QSFP56 is the same as QSFP28 MSA specification, with the module in compliance with the specifications in SFF-8679. Figure below shows the module connector pad layout, and table below lists and describes all of the electrical pins of the module.

ELECTRICAL CONNECTOR PAD LAYOUT



QSFP28 MODULE ELECTRICAL CONNECTOR PIN DEFINITIONS

PAD	LOGIC	SIC SYMBOL DESCRIPTION		PLUG SEQUENCE	NOTES
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		VccRx	+3.3V Power supply, receiver	2	2
11	LVCMOS-I/O	SCL	2 wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2 wire serial interface data	3	
13		GND	Ground	1	1
14	CML-0	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-0	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-0	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-0	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-0	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-0	Rx4n	Receiver Inverted Data Output	3	

QSFP28 MODULE ELECTRICAL CONNECTOR PIN DEFINITIONS CONT.

PAD	LOGIC	SYMBOL	DESCRIPTION	PLUG SEQUENCE	NOTES
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL/ RxLOS	Interrupt	3	
29		VccTx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	InitMode	Initialization mode; in legacy QSFP applications, this pad is called LPMode	3	
32		GND	Ground	1	1
33	CML-I	Тх3р	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Power Supply

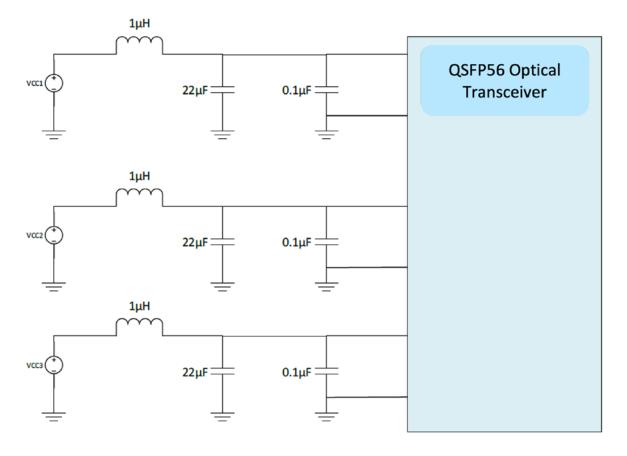
Here we describe the power supply filtering requirements and the power supply sequencing requirements.

POWER SUPPLY FILTERING

The power supply filtering requirements for the 200 Gbps FR4 QSFP56 Optical Transceiver have been designed to be consistent with those required for QSFP modules. A representative power supply filtering circuit is shown in figure below.

One filtering circuit is recommended for each power supply rail.

RECOMMENDED POWER SUPPLY FILTERING CIRCUIT



POWER SUPPLY SEQUENCING

No host power supply sequencing is required.

Control and Monitoring Interface

The 200 Gbps QSFP56 FR4 Optical Transceiver supports a full Hardware Pins support a full FR4 compliant set of control, alarm, and monitoring features through a standard I2C management interface as well as low speed control pins which support additional module control and interrupt features.

LOW-SPEED ELECTRICAL HARDWARE INTERFACE

In addition to the I²C interface, the optical transceiver also supports low speed control pins which provide immediate easy access to key module functions and provide additional user interface signals to support the management interface.

ResetL

ResetL (LVTTL-I signal) is an input pin. The ResetL pin has a weak pull-up in the module to Vcc. A low level on the ResetL pin for longer than the minimum pulse length (t_reset_init > 2µs) initiates a complete module reset and returns all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the "Low" level signal on the ResetL pin is released.

ModPrsL

ModPrsL (LVTTL-O signal) is pulled up to Vcc on the host board and grounded in the module. The ModPrsL pin is asserted "Low" when the module is inserted and deasserted "High" when the module is physically absent from the host connector.

IntL

IntL (LVTTL-O signal) is an output signal. When IntL is asserted "Low", it indicates a possible module operational fault, LOS condition or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface.

ModSelL

The ModSelL (LVTTL-I signal) is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. otherwise it does not. The ModSelL signal has a weak pull-up in the module connected to Vcc.

LPMode

LPMode (LVTTL-I signal) is an input signal. When LPMode is set "Low", the module will boot into its standard default state. When LPMode is set "High", the module will boot into 'low power mode' and only the management interface is active (high-speed TX and RX are shut down). The LPMode signal has a weak pull-up on the module connected to Vcc.

SCL

The SCL pin (LVCMOS-I/O open-drain signal) is the 2-wire serial interface clock for the module. The SCL signal requires a pull-up resistor on the host board, $\leq 3 \text{ k}\Omega$ is recommended. Note that SCL and SDA timing specifications are defined in section "Management interface timing".

SDA

The SDA pin (LVCMOS-I/O open-drain signal) is the 2-wire serial interface data for the module. The SDA signal requires a pull-up resistor on the host board, $\leq 3 \text{ k}\Omega$ is recommended. Note that SCL and SDA timing specifications are defined in section "Management interface timing".

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Management Interface

GENERAL FUNCTIONALITY

An I2C interface shall be used for management interface between the optical transceiver and the respective host systems. The communication protocol shall follow the industry standard and parameters specified by Facebook's QSFP-56 CMIS requirements. Timing specification for control and status follows SFF-8679 and in addition to these timing requirements are as listed below in reference to QSFP-DD Hardware Specification.

TIMING REQUIREMENTS FOR CONTROL AND STATUS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Mgmtlnit	t_init		2000	ms
Reset Init assert time	t_reset_init	10		μѕ
Serial bus hardware ready time	t_serial		2000	ms
Monitor data ready time	t_data		2000	ms
Reset assert time	t_reset		3000	ms
LPMode assert time	ton_LPMode	15	ms	
LPMode de-assert time	toff_LPMode	3000	ms	1
IntL assert time	ton_Intl		200	ms
IntL de-assert time	toff_Intl		7	ms
Rx LOS assert time	ton_LOS		100	ms
Tx fault assert time	ton_flag		200	ms
Flag assert time	toff_flag		200	ms
Mask assert time	ton_mask		100	ms
Mask de-assert time	toff mask		100	ms
Application or rate select change time	t ratesel		2000	ms
Power override or power set assert time	ton_Pdown		300	ms
Power override or power set deassert time	toff Pdown		2000	ms
Rx squelch assert time	ton_Rxsq		100	ms
Rx squelch de-assert time	toff_Rxsq		2000	ms

TIMING REQUIREMENTS FOR CONTROL AND STATUS CONT.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Tx squelch assert time	ton_Txsq		400	ms
Tx squelch de-assert time	toff_Txsq		2000	ms
Tx disable assert time	ton_txdis		3000	ms
Tx disable de-asssert time	toff_txdis		400	ms
Rx output disable assert time	ton_rxdis		100	ms
Rx output disable de-assert time	toff_rxdis		100	ms
Squelch disable assert time	ton_sqdis		100	ms
Squelch disable de-assert time	toff_sqdis		100	ms

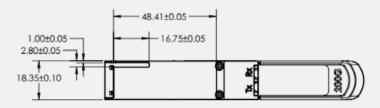
MONITOR ACCURACY

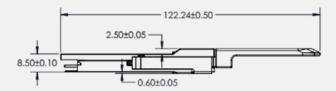
The module analog monitors have accuracy as defined below.

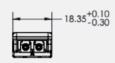
MONITOR	ACCURACY
RX input power monitor	+/- 3 dB
TX output power monitor	+/- 3 dB
TX bias current monitor	+/- 10%
Case temperature monitor	+/- 3C
Supply voltage monitor	+/- 10%

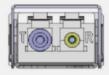
MECHANICAL SPECIFICATIONS

The module is compatible with the SFF-8661 specification. The module electrical connector is compliant with QSFP specifications. The module optical connector is a dual LC/UPC receptacle.









Label Specification

The following printed label is attached to the product (note that the certification labels will be added/removed according to requests and certification process results):

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QD2CIRLCCITOCL4 S/N: PJFRYYWWZZZZP 200G-FR4 2km 1311nm Class 1 Laser Product



Made in Vietnam

Regulatory and Compliance

EMC - Immunity

- EN 55024 (EU)
- IEC EN 61000-4-3 (International)
- EMC Directive 89/336/EEC
- IEC /CISPR/24

FMC - Fmission

- CISPR 22, class B (Comité International Spécial des Perturbations Radioélectriques--CISPR; Special international committee on radio interference. International).
- AS/NZS CISPR22 (Australia/New Zealand)
- · VCCI-03 (Japan)
- FCC 47 CFR Part 15, class B (US)
- ICES-003, Issue 4 (Canada)
- EN 55022 (EU)
- EMC Directive 2004/108/EEC (EU)

ESD Threshold

- Per MIL-STD 883C Method 3015.4 or ANSI/ESDA/JEDEC JS-001-2012 (component level).
- IEC EN 61000-4-2; +/- 8kV contact, +/- 15kV air.

Product Safety

- UL Recognized Component: UL 60950-1 (2nd Ed.) Information Technology Equipment; CAN/CSA-C22.2 No. 60950-1 (2007) Information Technology Equipment; UL94-V0 flammability.
- CB Certificate: IEC 60950-1 (2005 +A1:2009) Information Technology Equipment.

Fire Safety

- PCB material must be fully compliant to UL796; Temperature class B (IEC 60085); flammability class V-0- UL94).
- Cables and connectors must have a flammability ratings of V0- UL94; Service temp.≥90 C.
- Label materials must have a flammability ratings of V0- UL94; Service temp.≥90 C.
- Optical fibers must have a flammability ratings of V0- UL94; Service temp.≥85 C.

Optical Safety

- FDA/CDRH certified with accession number, Class 1 laser product:
- U.S. 21 CFR 1040;
- UL mark
- UL Certificate:
- IEC 60825-1:2014
- EN 60825-1:2014 + A11:2021

- Complies with 21 CFR 1040.10 and 1040.11 except for conformance with IEC 60825-1 Ed. 3., as described in Laser Notice No. 56, dated May 8, 2019.
- Caution Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

RoHS

- 2002/95/EC and the revised and recast Directive 2011/65/EC (RoHS) Restriction on Hazardous Substances.
- 2006/1907/EC (REACH) Registration, Evaluation, Authorization of Chemicals.
- JIG 101-A, JIG 101-B Joint Industry Guide Japanese Material Composition Declaration.
- CAITEC SJ/T 11363-2006 Requirements for Concentration Limits for Certain Hazardous Substances in Electronic Information Products (China RoHS).
- Complies with RoHS II Directive 2011/65/EU.

Ordering Information

JABIL PART NUMBER	PACKAGE	RATE	REACH	OTHER INFO
QD2CIRLCCxx0CL4	QSFP56	200G	2Km	C-Temp

Document Version

VERSION	DATE	NOTES
1.0	25/06/2024	Initial specification version
1.1	7/8/2024	Updated Regulatory and Compliance

Manufacturer's Address

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For additional information, visit jabil.com

About Jabil

At Jabil (NYSE: JBL), we are proud to be a trusted partner for the world's top brands, offering comprehensive engineering, manufacturing, and supply chain solutions. With over 50 years of experience across industries and a vast network of over 100 sites worldwide, Jabil combines global reach with local expertise to deliver both scalable and customized solutions. Our commitment extends beyond business success as we strive to build sustainable processes that minimize environmental impact and foster vibrant and diverse communities around the globe.

